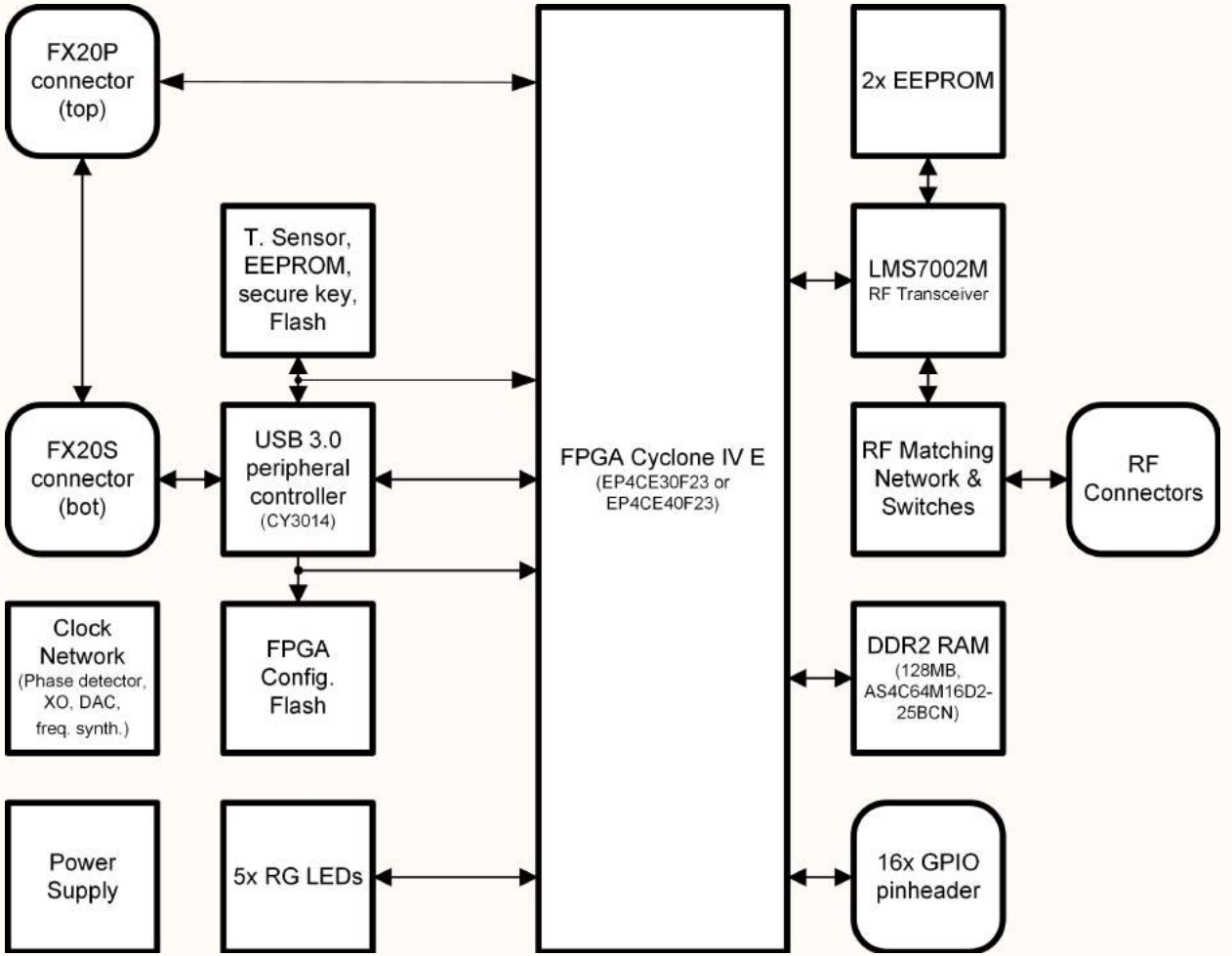
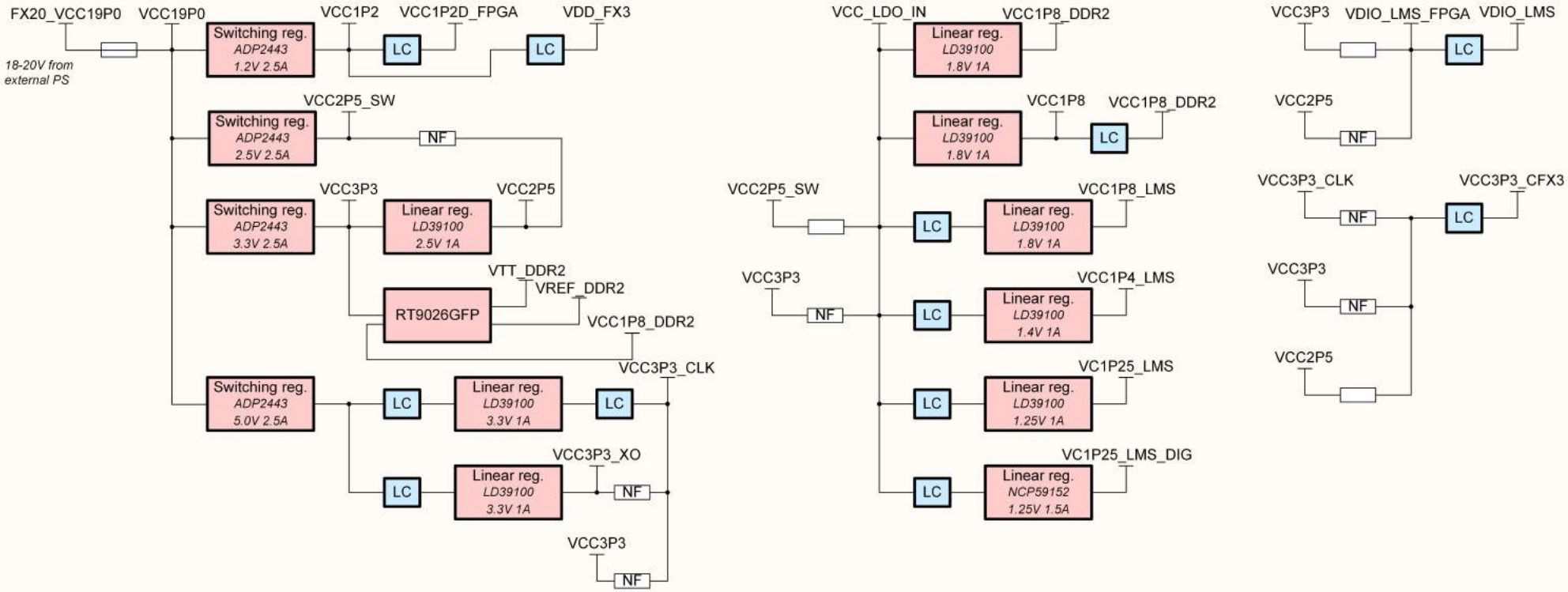
Block diagram



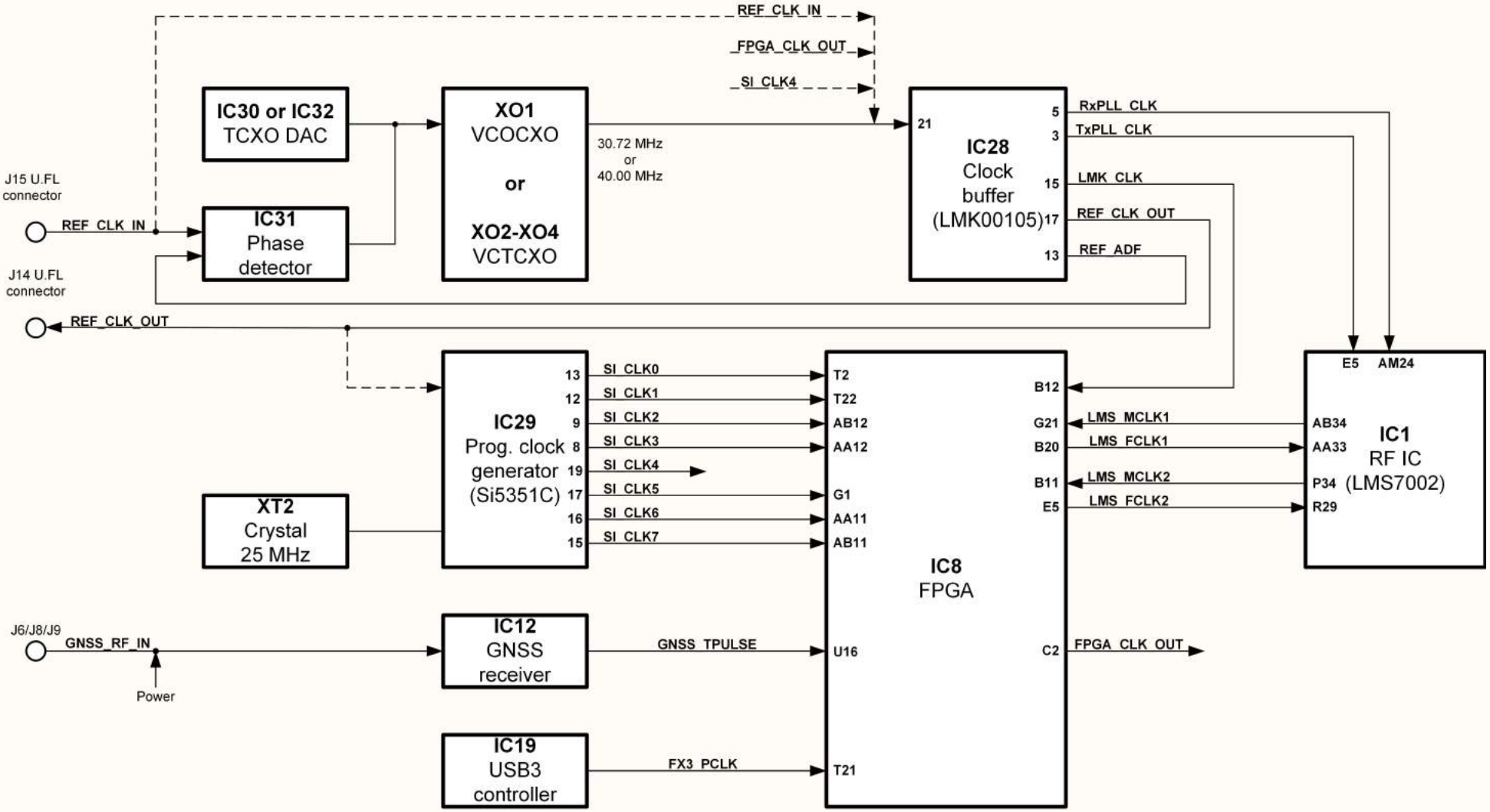
Project name: *LimeSDR-CORE_SDR_1v1.PrjPcb*			
Title: ***Block diagram***		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*	Lime microsystems
Size: A4	Revision: v1.1		
Date: 2018-11-28 Time: 10:50:43	Sheet1 of 16		
File: 01_BlockDiagram.SchDoc			

Power diagram



Project name: *LimeSDR-CORE_SDR_1v1.PrjPcb*			
Title: *Power diagram*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*	Lime microsystems
Size: A4	Revision: v1.1		
Date: 2018-11-28 Time: 10:50:51	Sheet2 of 16		
File: 02_PowerDiagram.SchDoc			

Clock diagram

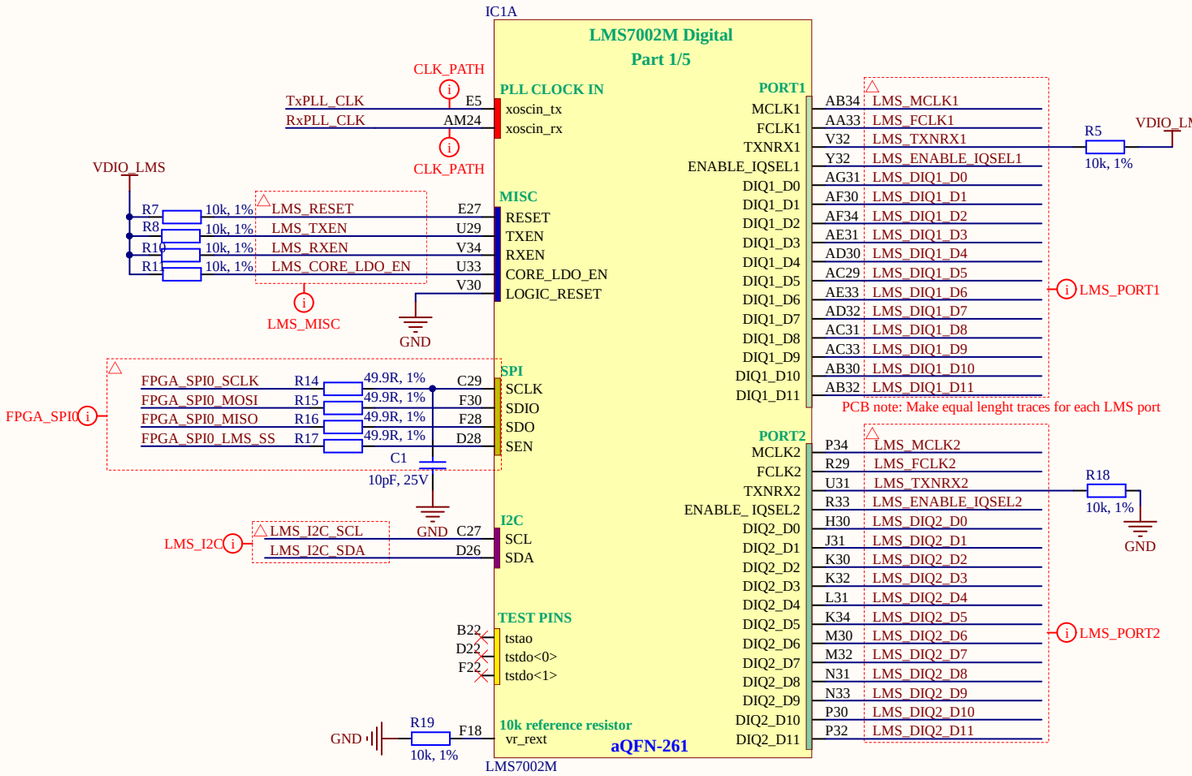


Project name: *LimeSDR-CORE_SDR_1v1.PrjPcb*			
Title: *Clock diagram*			*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A4	Revision: v1.1		
Date: 2018-11-28	Time: 10:51:06	Sheet3 of 16	
File: 03_ClockDiagram.SchDoc			

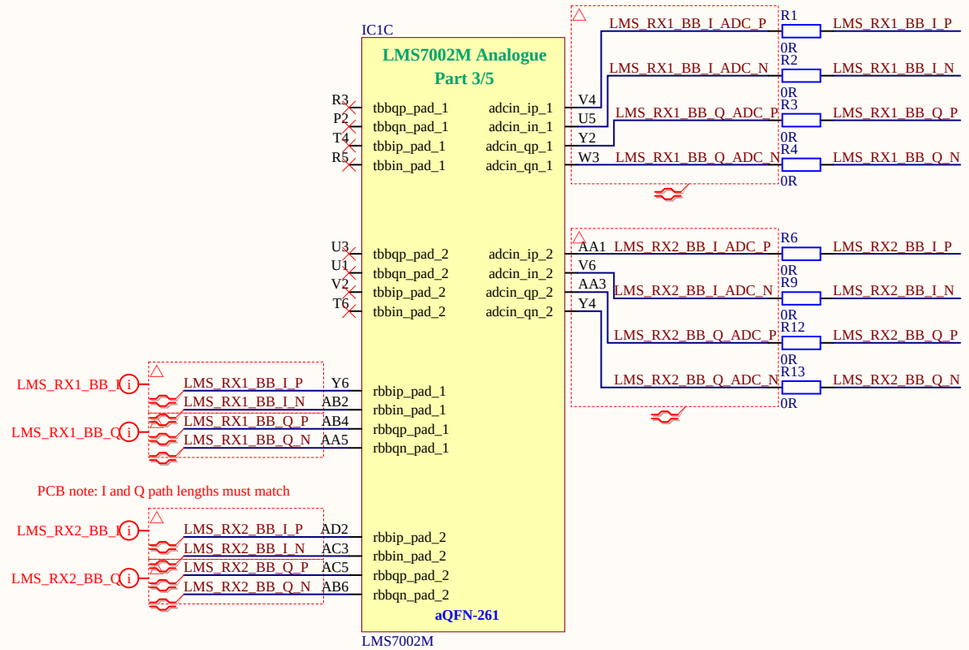
NF elements on sheet: -
Number of NF elements on sheet: 0

LMS7002M misc

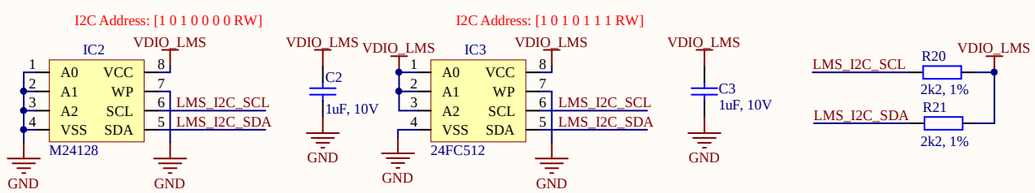
Digital interfaces



Baseband external IO



LMS EEPROMs



Project name:	*LimeSDR-CORE_SDR_1v1.PrjPcb*		
Title:	*LMS7002M misc*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2018-11-28	Time: 10:51:18	Sheet 4 of 16	
File: 04_LMS7002M_Misc.SchDoc			

NF elements on sheet: MN11, MN13, MN27, MN29, MN43, MN45, ESD1, ESD2
Number of NF elements on sheet: 8

LMS7002M RF circuits

RF Ch 1 (A)

RF Ch 2 (B)

IC1D — LMS7002M RF1 Part 4/5 (LMS7002M, aQFN-261)

TX1_1: pa1op_1 (B8), pa1on_1 (A7)
TX1_2: pa2op_1 (A9), pa2on_1 (B10)
RX1_L: rfgp_l_RFE_1 (AN11), rfgn_l_RFE_1 (AM12)
RX1_H: rfgp_h_RFE_1 (AK14), rfgn_h_RFE_1 (AJ15)
RX1_W: rfgp_w_RFE_1 (AN9), rfgn_w_RFE_1 (AP10)
rfsp_l_RFE_1 (AL13), rfsn_l_RFE_1 (AK12)

IC1E — LMS7002M RF2 Part 5/5 (LMS7002M, aQFN-261)

TX2_1: pa1op_2 (B12), pa1on_2 (C11)
TX2_2: pa2op_2 (A13), pa2on_2 (B14)
RX2_L: rfgp_l_RFE_2 (AN5), rfgn_l_RFE_2 (AP6)
RX2_H: rfgp_h_RFE_2 (AN7), rfgn_h_RFE_2 (AM8)
RX2_W: rfgp_w_RFE_2 (AN3), rfgn_w_RFE_2 (AM4)
rfsp_l_RFE_2 (AJ9), rfsn_l_RFE_2 (AJ7)

IC7 — PE42422

RF2, RF1, RFC, GND, GND, GND/NC, GND, GND, DGND, PAD, V1, LS, VDD

IC6 — SKY13345-368LF

RX1_H, RX1_W, RX1_L, RX1_V1, RX1_V2, RX1_V3, VCC3P3_RF, GND, VDD, GND, J1, J2, J3, V1, V2, V3, RFC, GND, N/C (GND), PAD

IC5 — PE42422

TX2_2, TX2_1, RF2, RF1, RFC, GND, GND, GND/NC, GND, GND, DGND, PAD, GND, V1, LS, VDD

IC4 — SKY13345-368LF

RX2_H, RX2_W, RX2_L, RX2_V1, RX2_V2, RX2_V3, VCC3P3_RF, GND, VDD, GND, J1, J2, J3, V1, V2, V3, RFC, GND, N/C (GND), PAD

Connectors

J1 MCX vertical — TX2
J2 MCX vertical — RX2
J3 MCX vertical — RX1
J4 MCX vertical — TX1

Transformers

T1, T2, T3, T4, T5, T6, T7, T8, T9, T10 — JA4220-AL_ (Secondary Primary 1:1)
TCM1-63AX+

Frequency bands

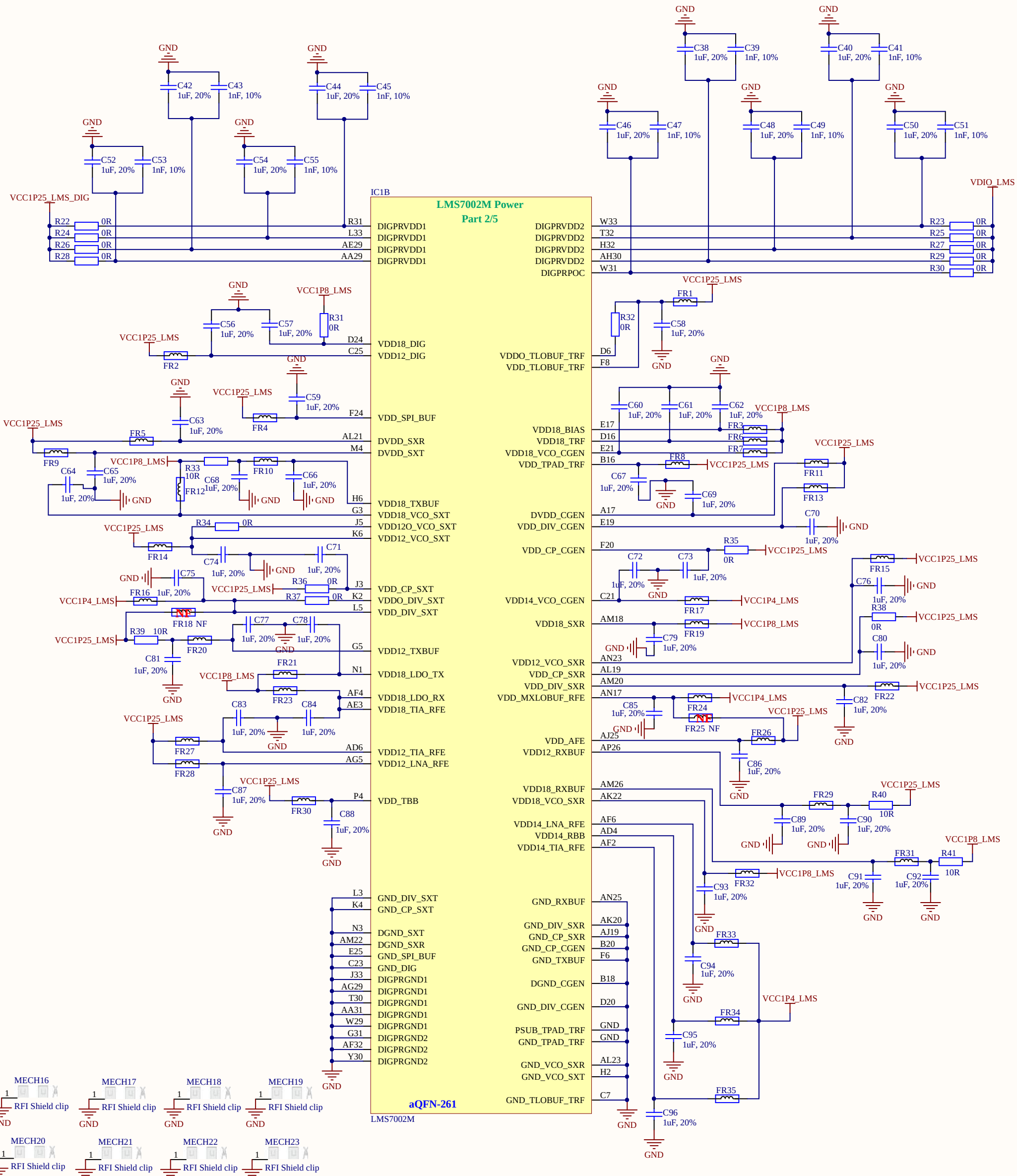
30 MHz - 1.9 GHz (TX1_1, TX2_1)
2 GHz - 2.6 GHz (TX1_2, TX2_2, RX1_H, RX2_H)
700 MHz - 2.6 GHz (RX1_L, RX1_W, RX2_L, RX2_W)

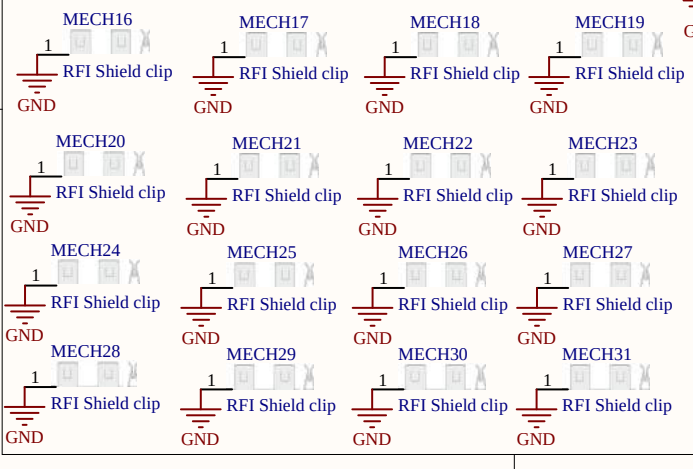
Project name:	LimeSDR-CORE_SDR_1v1.PrjPcb
Title:	LMS7002M RF
Size:	A3
Revision:	v1.1
Date:	2018-11-28
Time:	10:51:22
Sheet	5 of 16
File:	05_LMS7002M_RF.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

NF elements on sheet: FR18, FR25
Number of NF elements on sheet: 2

LMS7002M power supply circuit





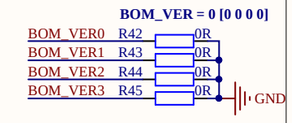
Project name:	LimeSDR-CORE_SDR_1v1.PrjPcb
Title:	LMS7002M power supply
Size:	A3
Revision:	v1.1
Date:	2018-11-28
Time:	10:51:27
Sheet	6 of 16
File:	06_LMS7002M_Power.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

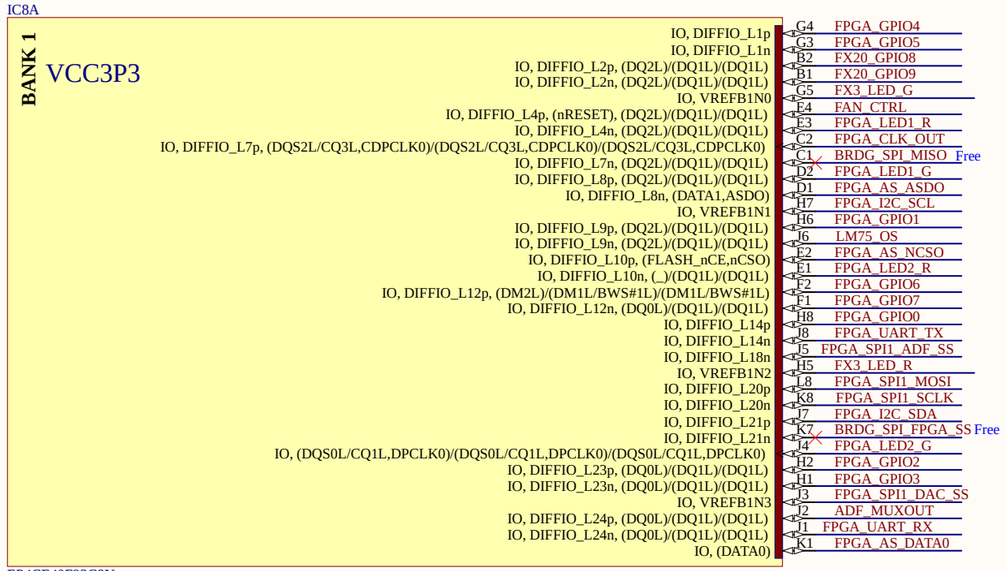
NF elements on sheet: R46
Number of NF elements on sheet: 1

FPGA banks 1, 2, 3, 4

BOM_VER = 0 [0 0 0 0]



IC8A



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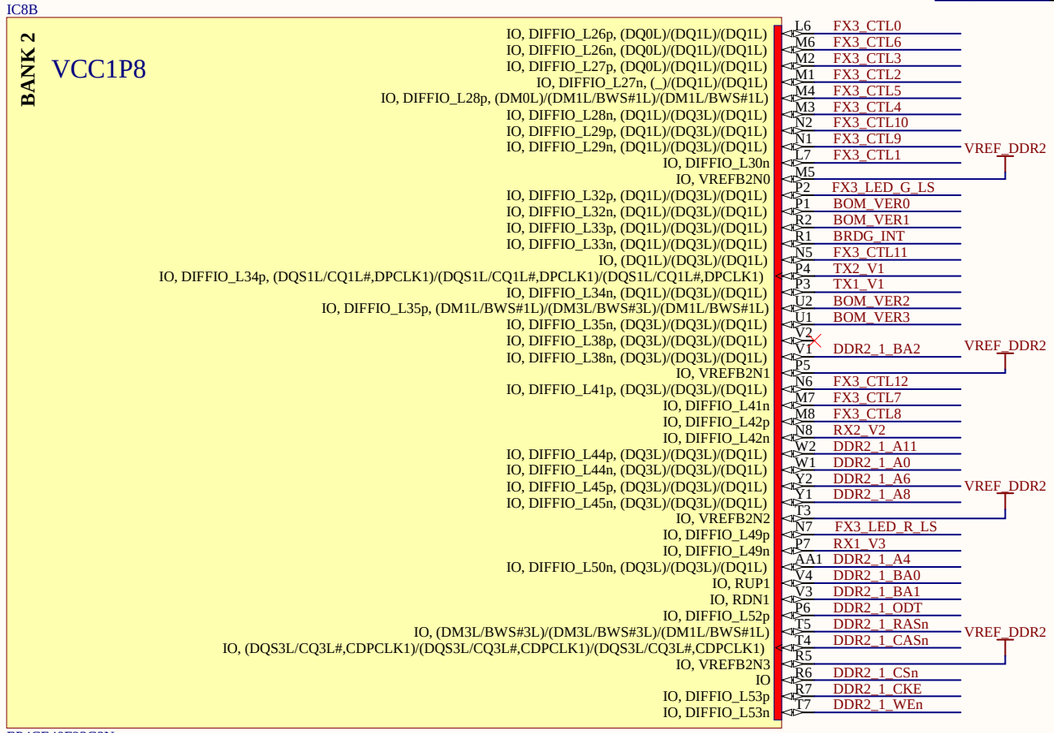
IC8B



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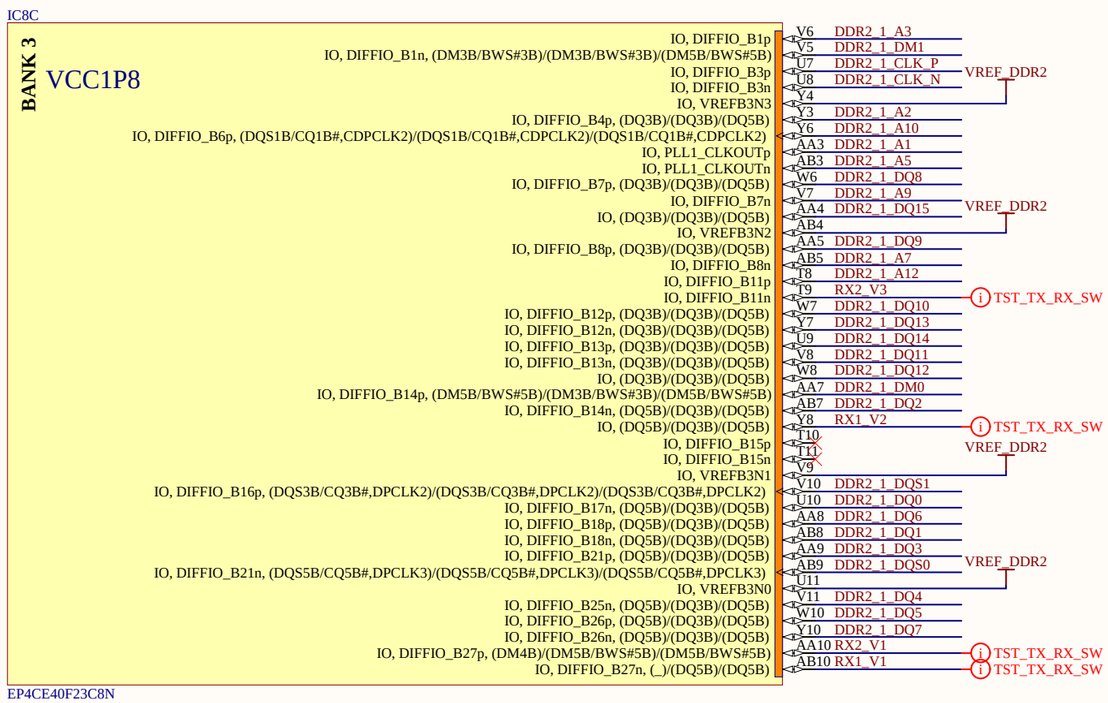
IC8C



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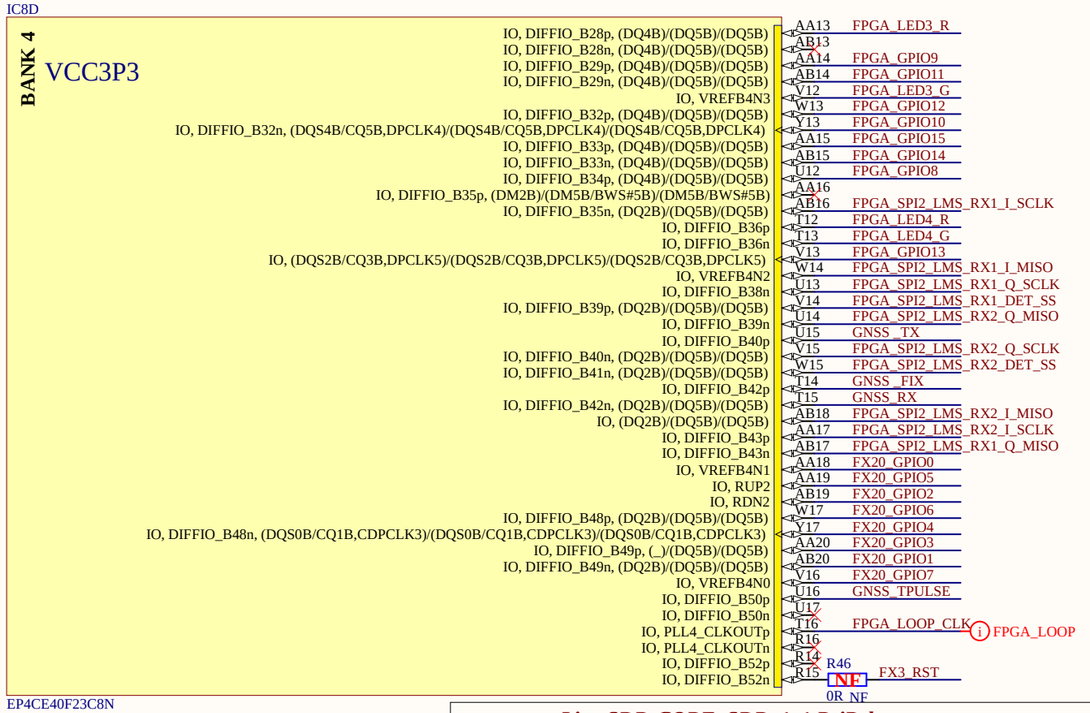
IC8D



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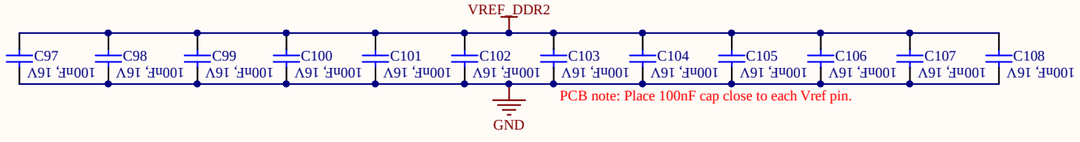

PCB note: Place 100nF cap close to each Vref pin.

Project name:	*LimeSDR-CORE_SDR_1v1.PrjPcb*		
Title:	*FPGA banks 1, 2, 3, 4*		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v1.1		
Date: 2018-11-28	Time: 10:51:33	Sheet 7 of 16	
File: 07_FPGA_banks_1_2_3_4.SchDoc			

NF elements on sheet: R47, R48
Number of NF elements on sheet: 2

FPGA banks 5, 6, 7, 8

IC8E

BANK 5 VCC1P8

IO, DIFFIO_R56p, (DM3R/BWS#3R)/(DM3R/BWS#3R)/(DM1R/BWS#1R)	AA21	FX3_DQ1
IO, RUP3	T17	
IO, RDN3	T18	GND
IO, (DQS3R/CQ3R#,CDPCLK4)/(DQS3R/CQ3R#,CDPCLK4)/(DQS3R/CQ3R#,CDPCLK4)	W20	FX3_DQ6
IO, VREFB5N3	W19	GND
IO, DIFFIO_R51n, (DQ3R)/(DQ3R)/(DQ1R)	Y22	FX3_DQ2
IO, DIFFIO_R51p	Y21	FX3_DQ3
IO, DIFFIO_R50n, (DQ3R)/(DQ3R)/(DQ1R)	U20	FX3_DQ11
IO, DIFFIO_R50p	U19	FX3_DQ12
IO, DIFFIO_R49n, (DQ3R)/(DQ3R)/(DQ1R)	W22	FX3_DQ4
IO, DIFFIO_R49p, (DQ3R)/(DQ3R)/(DQ1R)	W21	FX3_DQ5
IO, DIFFIO_R46n	P15	FX3_DQ24
IO, DIFFIO_R46p	P16	FX3_DQ23
IO, VREFB5N2	R17	GND
IO	P17	
IO, DIFFIO_R45n, (DQ3R)/(DQ3R)/(DQ1R)	V22	FX3_DQ7
IO, DIFFIO_R45p, (DQ3R)/(DQ3R)/(DQ1R)	V21	FX3_DQ8
IO, DIFFIO_R44n, (DQ3R)/(DQ3R)/(DQ1R)	R20	FX3_DQ17
IO, DIFFIO_R43n, (DQ3R)/(DQ3R)/(DQ1R)	U22	FX3_DQ9
IO, DIFFIO_R43p, (DQ3R)/(DQ3R)/(DQ1R)	U21	FX3_DQ10
IO, DIFFIO_R42n	R18	FX3_DQ19
IO, DIFFIO_R42p, (DM1R/BWS#1R)/(DM3R/BWS#3R)/(DM1R/BWS#1R)	R19	FX3_DQ18
IO, DIFFIO_R40p	N16	FX3_DQ31
IO, DIFFIO_R39n, (DQ1R)/(DQ3R)/(DQ1R)	R22	FX3_DQ15
IO, DIFFIO_R39p, (DQ1R)/(DQ3R)/(DQ1R)	R21	FX3_DQ16
IO, VREFB5N1	P20	GND
IO, DIFFIO_R38n, (DQ1R)/(DQ3R)/(DQ1R)	P22	FX3_DQ20
IO, DIFFIO_R38p, (DQ1R)/(DQ3R)/(DQ1R)	P21	FX3_DQ21
IO, DIFFIO_R36n, (DQ1R)/(DQ3R)/(DQ1R)	N20	FX3_DQ27
IO, DIFFIO_R36p	N19	FX3_DQ28
IO, DIFFIO_R33n	N17	FX3_DQ30
IO, DIFFIO_R33p, (DQS1R/CQ1R#,DPCLK6)/(DQS1R/CQ1R#,DPCLK6)/(DQS1R/CQ1R#,DPCLK6)	N18	FX3_DQ29
IO, DIFFIO_R32n, (DEV_OE)	N22	FX3_DQ25
IO, DIFFIO_R32p, (DEV_CLRn)	N21	FX3_DQ26
IO, DIFFIO_R31n, (DQ1R)/(DQ3R)/(DQ1R)	M22	FX3_DQ13
IO, DIFFIO_R31p, (DQ1R)/(DQ3R)/(DQ1R)	M21	FX3_DQ14
IO, DIFFIO_R30n, (DQ1R)/(DQ3R)/(DQ1R)	M20	FX3_DQ22
IO, DIFFIO_R30p, (DQ1R)/(DQ3R)/(DQ1R)	M19	FX3_DQ0
IO, VREFB5N0	M16	GND

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IC8F

BANK 6 VDIO_LMS_FPGA

IO, DIFFIO_R27n, (INIT_DONE)	L22	
IO, DIFFIO_R27p, (CRC_ERROR)	L21	
IO, VREFB6N3	K19	GND
IO, DIFFIO_R24n, (nCEO)	K22	
IO, DIFFIO_R24p, (CLKUSR)	K21	
IO, DIFFIO_R23n, (DQS0R/CQ1R,DPCLK7)/(DQS0R/CQ1R,DPCLK7)/(DQS0R/CQ1R,DPCLK7)	J22	
IO, DIFFIO_R23p, (DM0R)/(DM1R/BWS#1R)/(DM1R/BWS#1R)	J21	
IO, DIFFIO_R22n, (DQ0R)/(DQ1R)/(DQ1R)	H22	
IO, DIFFIO_R22p, (DQ0R)/(DQ1R)/(DQ1R)	H21	
IO, DIFFIO_R20n	K17	
IO, DIFFIO_R20p, (DQ0R)/(DQ1R)/(DQ1R)	K18	
IO, VREFB6N2	J18	GND
IO, DIFFIO_R18n, (DQ0R)/(DQ1R)/(DQ1R)	F22	FPGA_SW2
IO, DIFFIO_R18p, (DQ0R)/(DQ1R)/(DQ1R)	F21	FPGA_SW3
IO, DIFFIO_R13n, (DQ0R)/(DQ1R)/(DQ1R)	H20	
IO, DIFFIO_R13p, (DQ0R)/(DQ1R)/(DQ1R)	H19	
IO, DIFFIO_R12n, (nWE), (DQ0R)/(DQ1R)/(DQ1R)	F22	
IO, DIFFIO_R12p, (nOE), (_)/(DQ1R)/(DQ1R)	F21	
IO, VREFB6N1	H18	GND
IO, DIFFIO_R10n	J17	
IO, DIFFIO_R10p	H16	
IO, DIFFIO_R9n, (DM2R)/(DM1R/BWS#1R)/(DM1R/BWS#1R)	D22	FPGA_SW0
IO, DIFFIO_R9p, (_)/(DQ1R)/(DQ1R)	D21	FPGA_SW1
IO, DIFFIO_R8n, (nAVD), (DQ2R)/(DQ1R)/(DQ1R)	F20	HW_VER0
IO, DIFFIO_R8p, (DQ2R)/(DQ1R)/(DQ1R)	F19	HW_VER1
IO, DIFFIO_R7n, (PADD23), (DQ2R)/(DQ1R)/(DQ1R)	G18	HW_VER2
IO, DIFFIO_R7p	H17	HW_VER3
IO, DIFFIO_R6n, (DQ2R)/(DQ1R)/(DQ1R)	C22	
IO, DIFFIO_R6p, (DQ2R)/(DQ1R)/(DQ1R)	C21	LMS_I2C_SDA
IO, DIFFIO_R5n, (PADD22), (DQ2R)/(DQ1R)/(DQ1R)	B22	
IO, DIFFIO_R5p, (PADD21), (DQ2R)/(DQ1R)/(DQ1R)	B21	
IO, DIFFIO_R4n, (PADD20), (DQS2R/CQ3R,CDPCLK5)/(DQS2R/CQ3R,CDPCLK5)/(DQS2R/CQ3R,CDPCLK5)	C20	
IO, VREFB6N0	D20	GND
IO, DIFFIO_R2n, (DQ2R)/(DQ1R)/(DQ1R)	F17	
IO, DIFFIO_R2p	G17	

GND, GND, GND

HW_VER = 0 [0 0 0 1]

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FPGA_LOOP

IC8G

BANK 7 VDIO_LMS_FPGA

IO, DIFFIO_T51n	F16	FPGA_LOOP_D0
IO, DIFFIO_T51p, (DQ2T)/(DQ5T)/(DQ5T)	E16	
IO, DIFFIO_T50n, (DQ2T)/(DQ5T)/(DQ5T)	F15	FPGA_LOOP_D1
IO, DIFFIO_T50p	G16	
IO, DIFFIO_T49n	G15	FPGA_LOOP_D3
IO, DIFFIO_T49p, (DQS0T/CQ1T,CDPCLK6)/(DQS0T/CQ1T,CDPCLK6)/(DQS0T/CQ1T,CDPCLK6)	F14	
IO, DIFFIO_T48n	H15	FPGA_LOOP_D0
IO, DIFFIO_T48p	H14	FPGA_LOOP_D1
IO, VREFB7N0	D17	GND
IO, DIFFIO_T47n, (DQ2T)/(DQ5T)/(DQ5T)	C19	R47 NF FX3_I2C_SDA
IO, DIFFIO_T47p, (DQ2T)/(DQ5T)/(DQ5T)	D19	
IO, PLL2_CLKOUTn	A20	R48 0R NF FX3_I2C_SCL
IO, PLL2_CLKOUTp	B20	LMS_FCLK1
IO, DIFFIO_T46p, (DQ2T)/(DQ5T)/(DQ5T)	C17	LMS_I2C_SCL
IO, RUP4	B19	
IO, RDN4	A19	GND
IO, DIFFIO_T45n, (DQ2T)/(DQ5T)/(DQ5T)	A18	LMS_DIQ1_D6
IO, DIFFIO_T45p, (PADD0)	B18	LMS_CORE_LDO_EN
IO, VREFB7N1	D15	GND
IO, DIFFIO_T44n, (DQ2T)/(DQ5T)/(DQ5T)	E15	
IO, DIFFIO_T44p	G14	
IO, DIFFIO_T42n	G13	
IO, DIFFIO_T41n, (PADD1), (DQ2T)/(DQ5T)/(DQ5T)	A17	LMS_DIQ1_D7
IO, DIFFIO_T41p, (PADD2), (_)/(DQ5T)/(DQ5T)	B17	LMS_DIQ1_D0
IO, DIFFIO_T40n, (DM2T)/(DM5T/BWS#5T)/(DM5T/BWS#5T)	A16	LMS_DIQ1_D8
IO, DIFFIO_T40p, (DQ4T)/(DQ5T)/(DQ5T)	B16	LMS_DIQ1_D1
IO, VREFB7N2	C15	GND
IO, DIFFIO_T38n, (PADD3), (DQ4T)/(DQ5T)/(DQ5T)	E14	FPGA_LOOP_D3
IO, DIFFIO_T37p, (PADD4), (DQS2T/CQ3T,DPCLK8)/(DQS2T/CQ3T,DPCLK8)/(DQS2T/CQ3T,DPCLK8)	F13	
IO, DIFFIO_T36n, (PADD5), (DQ4T)/(DQ5T)/(DQ5T)	A15	LMS_DIQ1_D9
IO, DIFFIO_T36p, (PADD6), (DQ4T)/(DQ5T)/(DQ5T)	B15	LMS_DIQ1_D2
IO, DIFFIO_T35n, (PADD7)	C13	LMS_DIQ1_D5
IO, DIFFIO_T35p, (PADD8), (DQ4T)/(DQ5T)/(DQ5T)	D13	
IO, VREFB7N3	E13	GND
IO, DIFFIO_T31n, (PADD9), (DQ4T)/(DQ5T)/(DQ5T)	A14	LMS_DIQ1_D10
IO, DIFFIO_T31p, (PADD10), (DQ4T)/(DQ5T)/(DQ5T)	B14	LMS_DIQ1_D3
IO, DIFFIO_T29n, (PADD11), (DQ4T)/(DQ5T)/(DQ5T)	A13	LMS_DIQ1_D11
IO, DIFFIO_T29p, (PADD12), (DQS4T/CQ5T,DPCLK9)/(DQS4T/CQ5T,DPCLK9)/(DQS4T/CQ5T,DPCLK9)	B13	LMS_DIQ1_D4
IO, DIFFIO_T28p, (_)/(DQ5T)/(DQ5T)	E12	
IO, DIFFIO_T27n, (PADD13)	E11	
IO, DIFFIO_T27p, (PADD14), (DM4T)/(DM5T/BWS#5T)/(DM5T/BWS#5T)	F11	FPGA_LOOP_D2

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IC8H

BANK 8 VDIO_LMS_FPGA

IO, DIFFIO_T26n, (DQ5T)/(DQ3T)/(DQ5T)	D10	FPGA_SPI0_LMS_SS
IO, DIFFIO_T26p	E10	
IO, DIFFIO_T25n, (DQ5T)/(DQ3T)/(DQ5T)	A10	LMS_DIQ2_D4
IO, DIFFIO_T25p, (PADD15)	B10	LMS_TXEN
IO, DIFFIO_T24n, (PADD16), (DQ5T)/(DQ3T)/(DQ5T)	A9	LMS_DIQ2_D5
IO, DIFFIO_T24p, (PADD17), (DQS5T/CQ5T#,DPCLK10)/(DQS5T/CQ5T#,DPCLK10)/(DQS5T/CQ5T#,DPCLK10)	B9	LMS_TXNRX1
IO, VREFB8N0	C10	GND
IO, DIFFIO_T22n	G11	
IO, DIFFIO_T20n, (DATA2), (DQ5T)/(DQ3T)/(DQ5T)	A8	LMS_DIQ2_D6
IO, DIFFIO_T20p, (DATA3), (DQ5T)/(DQ3T)/(DQ5T)	B8	LMS_TXNRX2
IO, DIFFIO_T19n, (PADD18), (DQ5T)/(DQ3T)/(DQ5T)	A7	LMS_DIQ2_D7
IO, DIFFIO_T19p, (DATA4), (DQ5T)/(DQ3T)/(DQ5T)	B7	LMS_DIQ2_D0
IO, DIFFIO_T18n, (PADD19), (DQ5T)/(DQ3T)/(DQ5T)	A6	LMS_DIQ2_D8
IO, DIFFIO_T18p, (DATA15), (DQ5T)/(DQ3T)/(DQ5T)	B6	LMS_DIQ2_D1
IO, VREFB8N1	E9	GND
IO, DIFFIO_T16n, (DATA14), (DQS3T/CQ3T#,DPCLK11)/(DQS3T/CQ3T#,DPCLK11)/(DQS3T/CQ3T#,DPCLK11)	C8	FPGA_SPI0_MISO
IO, DIFFIO_T16p, (DATA13), (DM5T/BWS#5T)/(DM3T/BWS#3T)/(DM5T/BWS#5T)	C7	LMS_ENABLE_IQSEL2
IO, DIFFIO_T14n	H11	FPGA_LOOP_D2
IO, DIFFIO_T14p	H10	
IO, DIFFIO_T11p, (DATA5), (DQ3T)/(DQ3T)/(DQ5T)	A5	LMS_DIQ2_D9
IO, VREFB8N2	B5	GND
IO, DIFFIO_T8n	G10	
IO, DIFFIO_T8p, (DATA6), (DQ3T)/(DQ3T)/(DQ5T)	F10	
IO, DIFFIO_T7n, (DATA7), (DQ3T)/(DQ3T)/(DQ5T)	C6	LMS_RESET
IO, DIFFIO_T7p	D7	FPGA_SPI0_MOSI
IO, DIFFIO_T6n, (DQ3T)/(DQ3T)/(DQ5T)	A4	LMS_DIQ2_D10
IO, DIFFIO_T6p, (DATA8), (DQ3T)/(DQ3T)/(DQ5T)	B4	LMS_DIQ2_D2
IO, DIFFIO_T5n, (DATA9), (DQ3T)/(DQ3T)/(DQ5T)	F8	
IO, DIFFIO_T5p	G8	
IO, DIFFIO_T4n, (DATA10), (DQ3T)/(DQ3T)/(DQ5T)	A3	LMS_DIQ2_D11
IO, DIFFIO_T4p, (DATA11), (DQ3T)/(DQ3T)/(DQ5T)	B3	LMS_DIQ2_D3
IO, VREFB8N3	D6	GND
IO	F7	
IO, DIFFIO_T3n, (DQ3T)/(DQ3T)/(DQ5T)	C3	LMS_RXEN
IO, DIFFIO_T3p, (DATA12), (DQS1T/CQ1T#,CDPCLK7)/(DQS1T/CQ1T#,CDPCLK7)/(DQS1T/CQ1T#,CDPCLK7)	C4	LMS_ENABLE_IQSEL1
IO, DIFFIO_T1n, (DM3T/BWS#3T)/(DM3T/BWS#3T)/(DM5T/BWS#5T)	F7	
IO, DIFFIO_T1p	G7	
IO	F9	
IO, PLL3_CLKOUTn	F6	FPGA_SPI0_SCLK
IO, PLL3_CLKOUTp	E5	LMS_FCLK2
IO	G9	

EP4CE40F23C8N

Project name:	LimeSDR-CORE_SDR_1v1.PrjPcb
Title:	FPGA banks 5, 6, 7, 8
Size: A3	Revision: v1.1
Date: 2018-11-28	Time: 10:51:37 Sheet 8 of 16
File:	08_FPGA_banks_5_6_7_8.SchDoc

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

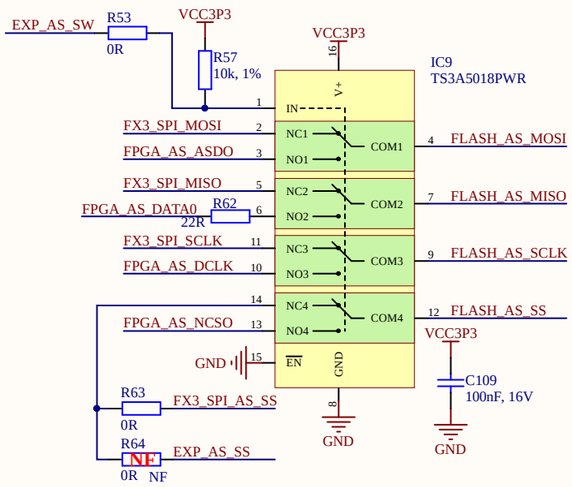
Lime microsystems

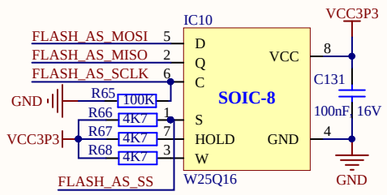
NF elements on sheet: R50, R51, R56, R60, R63, C137
Number of NF elements on sheet: 6

FPGA misc (power, clocks, config)

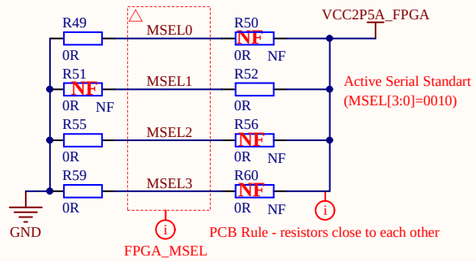
FPGA AS FLASH + Switch

IN:
0: FLASH conneccted to FX3 (NC to COM)
1: FLASH conneccted to FPGA (NO to COM)



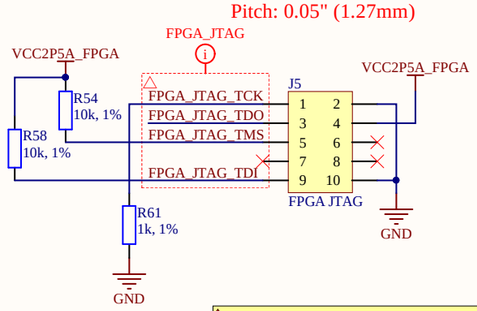


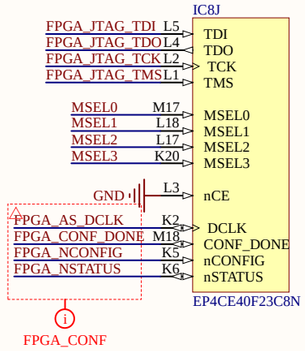
MSEL config

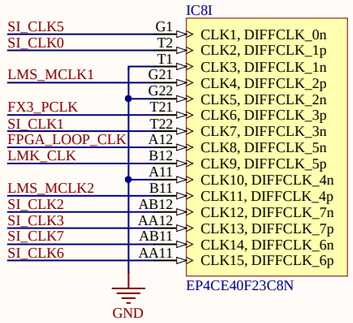


FPGA JTAG

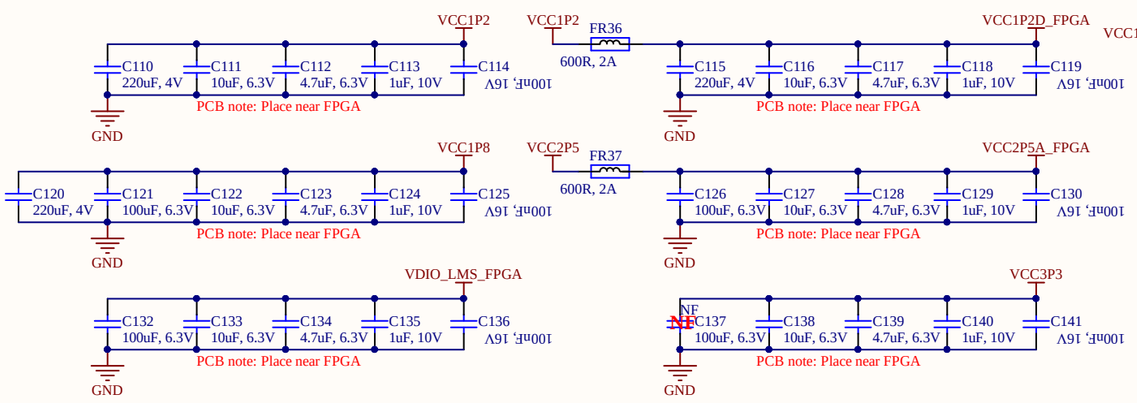
Pitch: 0.05" (1.27mm)



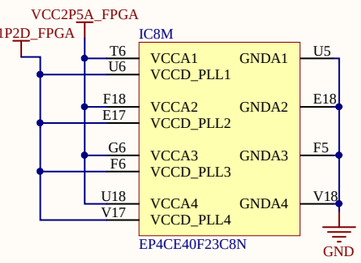


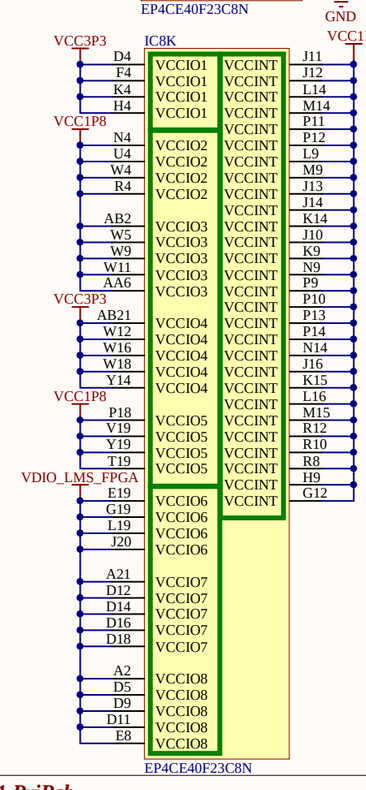


FPGA Bulk caps

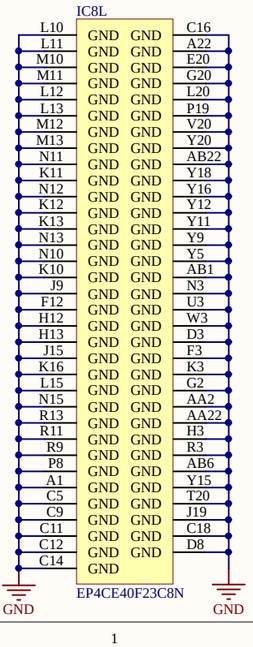


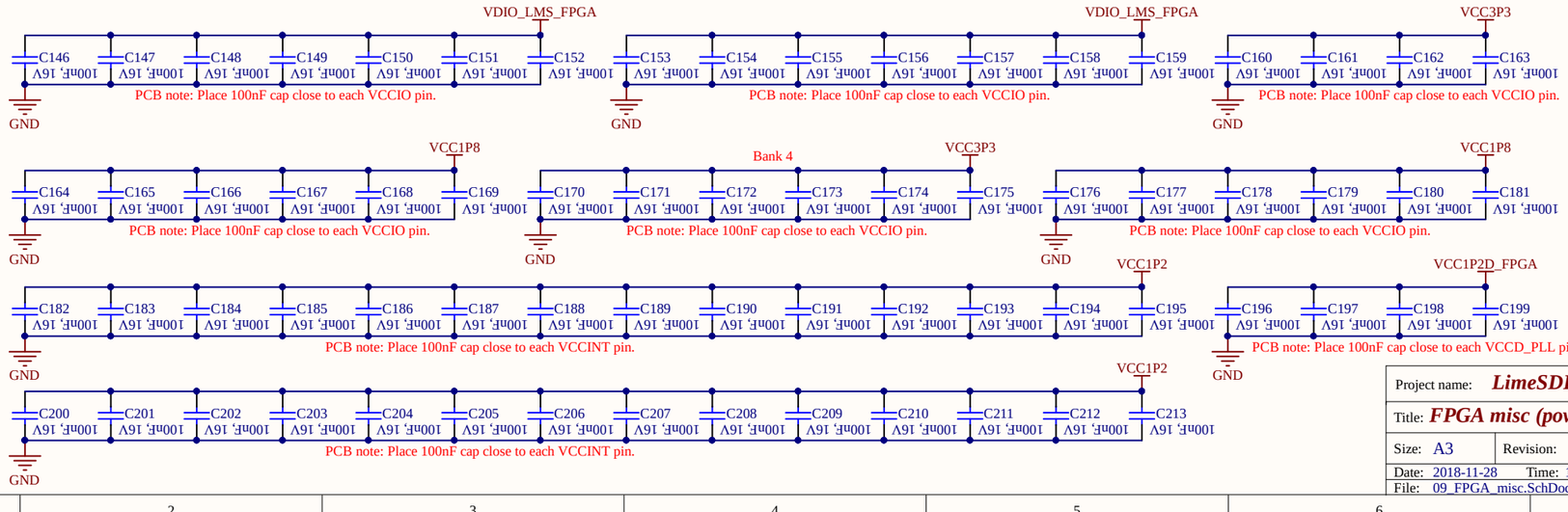
FPGA Power





FPGA Decoupling caps





Project name:	*LimeSDR-CORE_SDR_1v1.PrjPcb*		
Title:	*FPGA misc (power, clocks, config)*		
Size: A3	Revision: v1.1		
Date: 2018-11-28	Time: 10:51:42	Sheet 9 of 16	
File: 09_FPGA_misc.SchDoc			

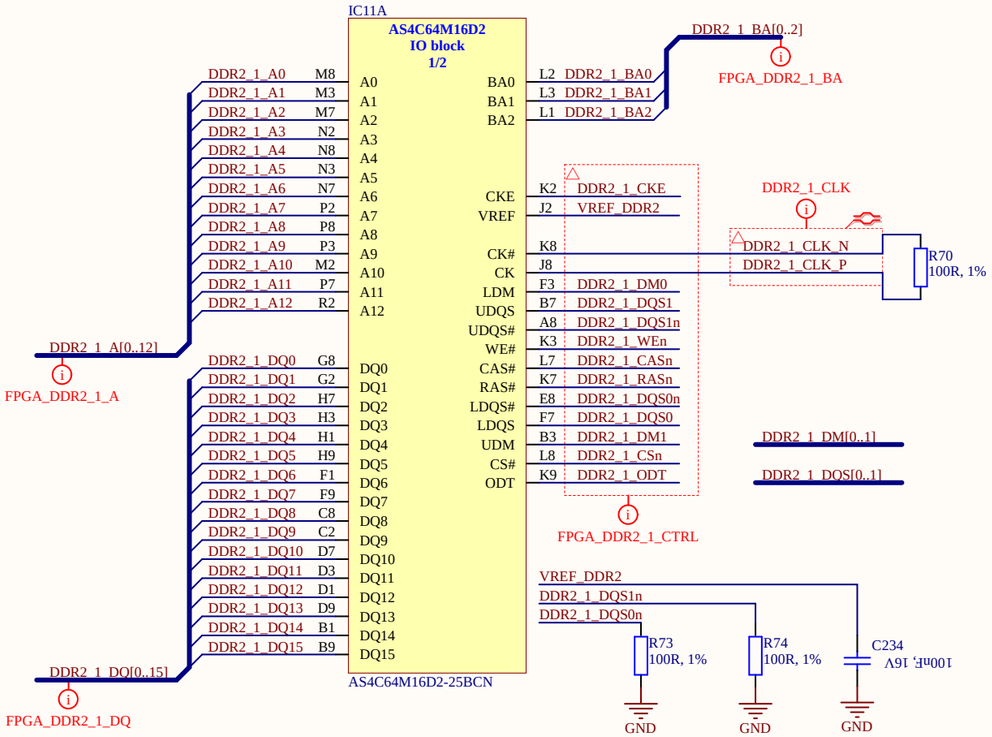
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

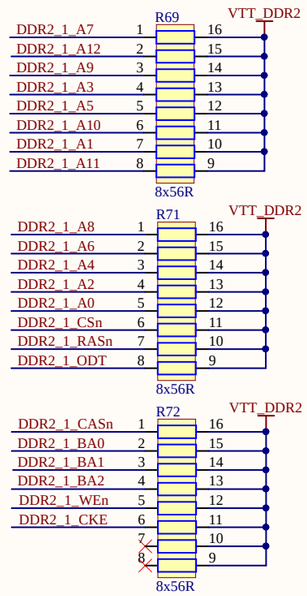
Lime microsystems

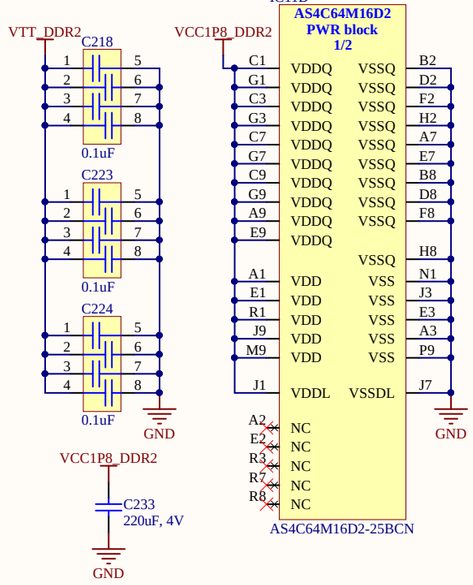
NF elements on sheet: R87, R89, R93, R95, R96, R99, R102, R300, J8, J9, ESD3
Number of NF elements on sheet: 11

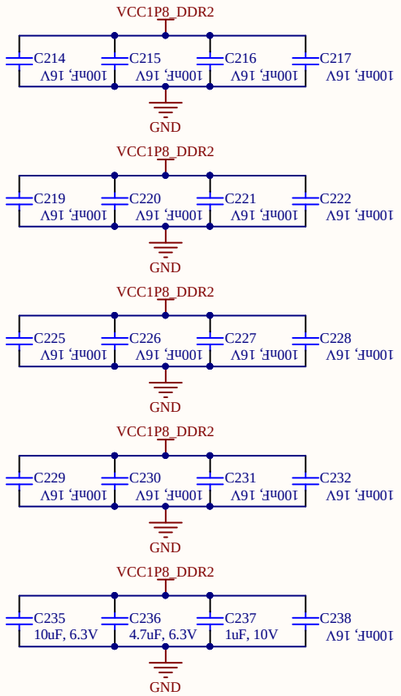
Peripherals

DDR2_1 (BOT L)

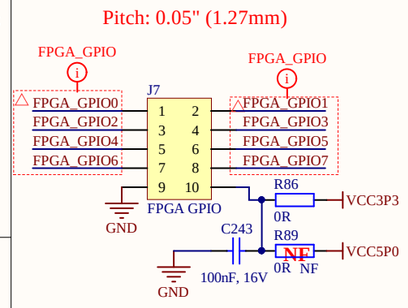


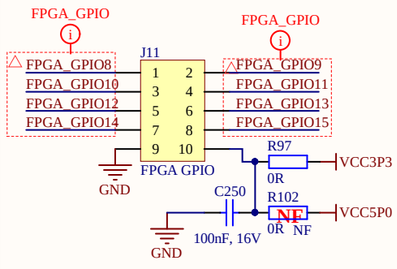




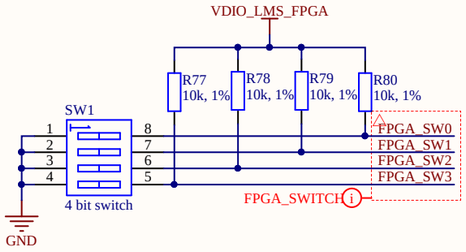


FPGA GPIO

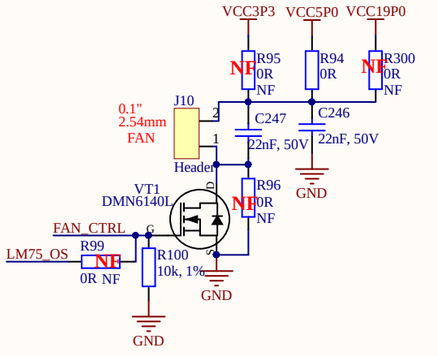




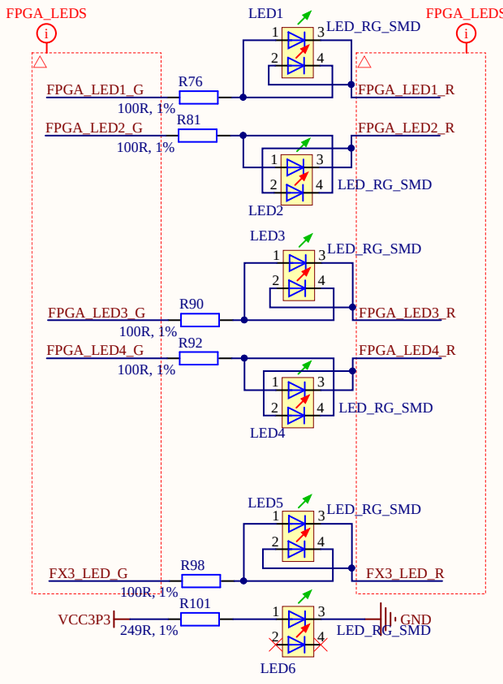
FPGA_SW



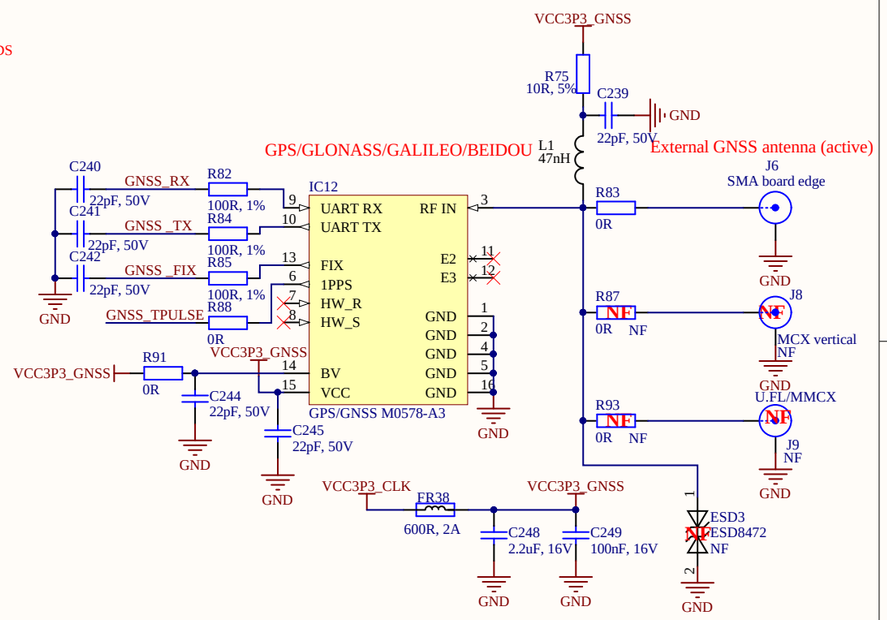
FAN control



FPGA LEDs



GNSS receiver



Project name:	*LimeSDR-CORE_SDR_1v1.PrjPcb*
Title:	*Peripherals*
Size:	A3
Revision:	v1.1
Date:	2018-11-28
Time:	10:51:48
Sheet	10 of 16
File:	10_Peripherals.SchDoc

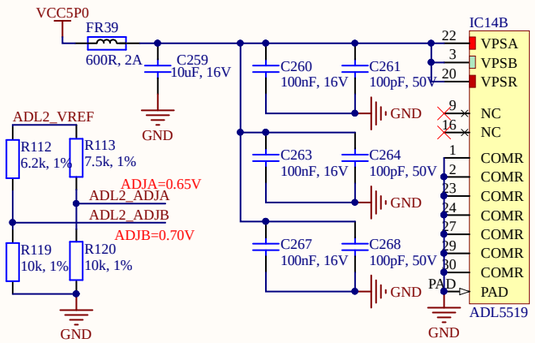
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surray
United Kingdom

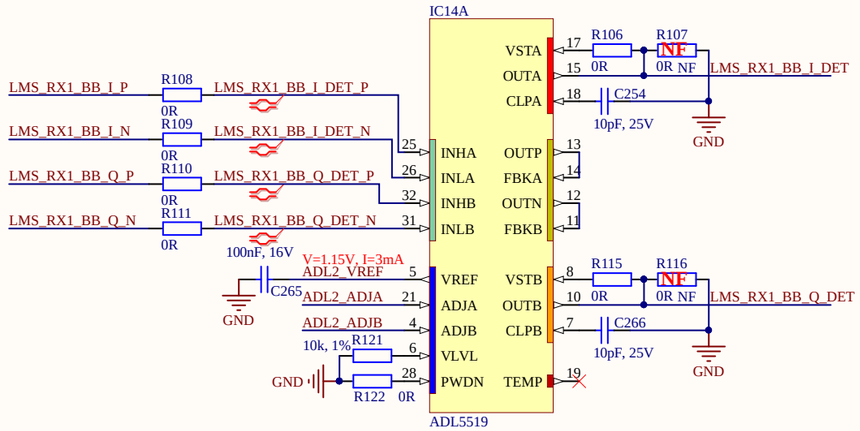
Lime microsystems

NF elements on sheet: C251, R107, C262, R116, C275, R127, C286, R135
Number of NF elements on sheet: 8

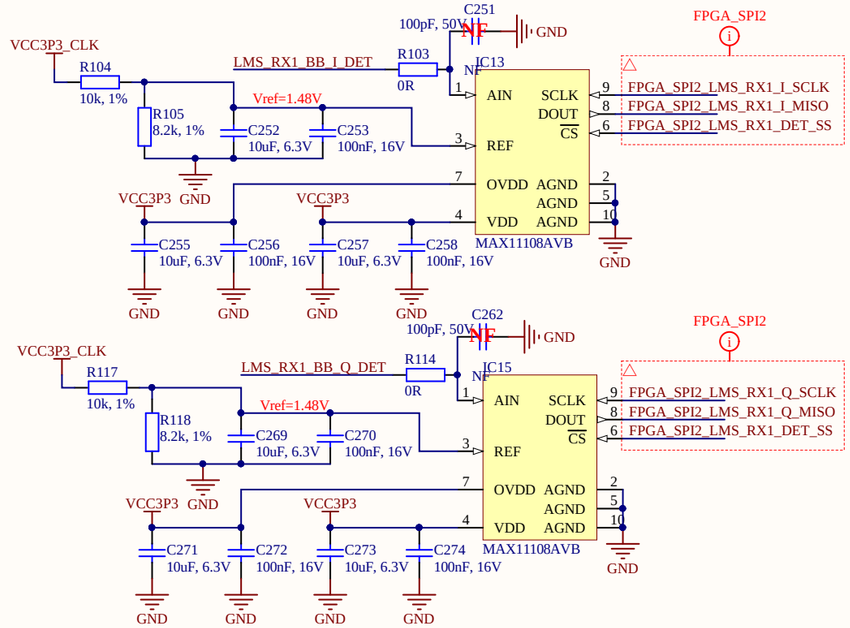
Log Detector

LMS_RX1_BB



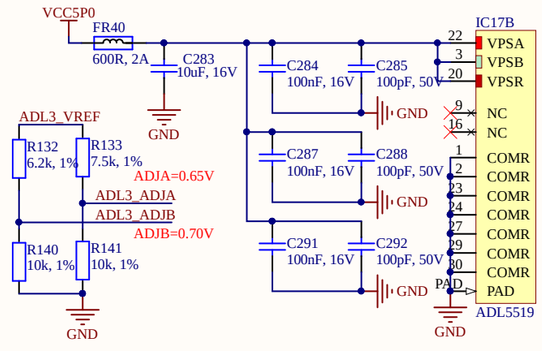


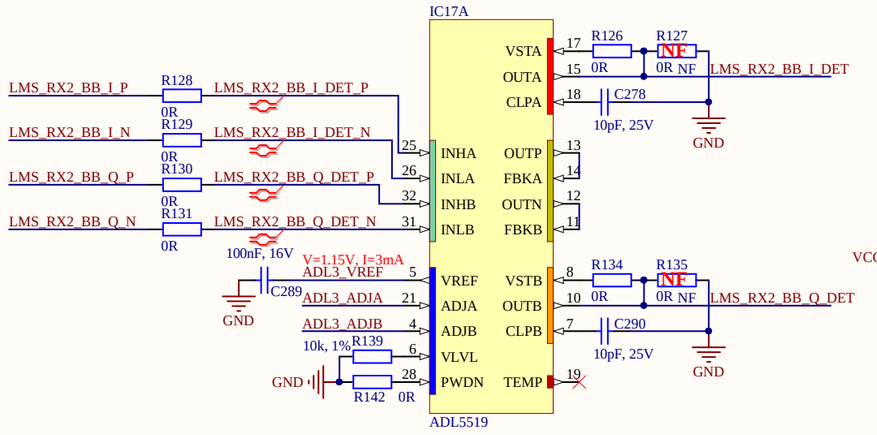
ADC



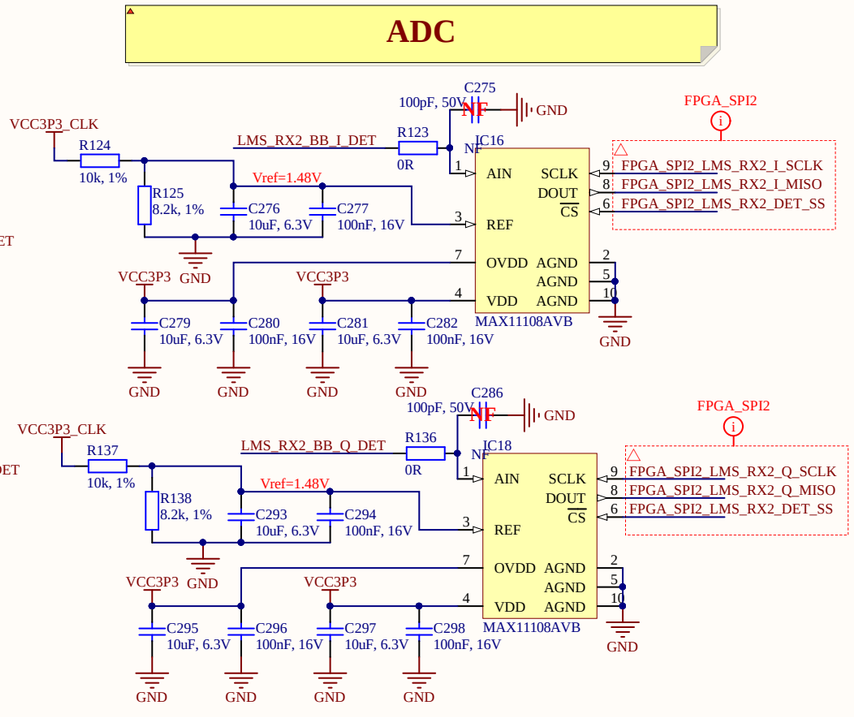
Log Detector

LMS_RX2_BB





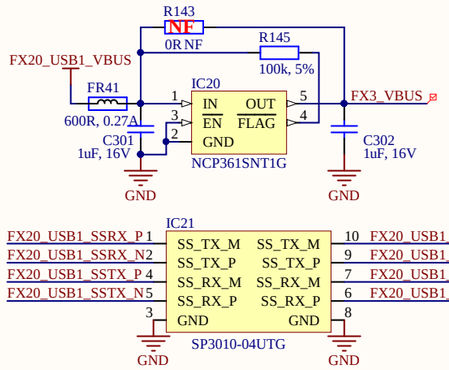
ADC

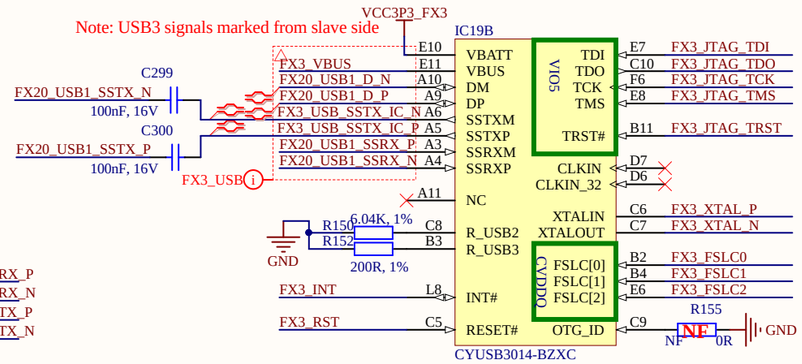


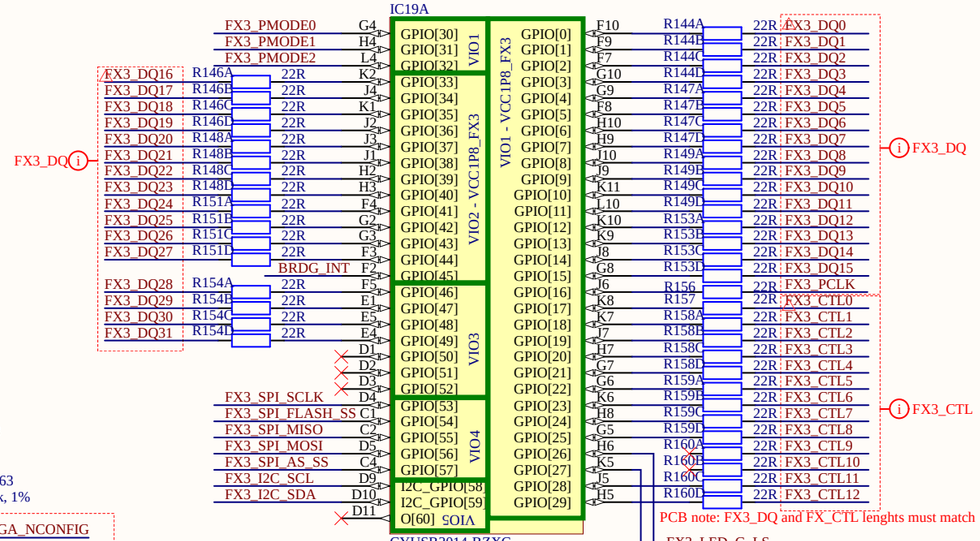
Project name:	*LimeSDR-CORE_SDR_1v1.PrjPcb*		
Title:	*RSSI*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2018-11-28	Time: 10:51:54	Sheet 11 of 16	
File: 11_RSSI.SchDoc			

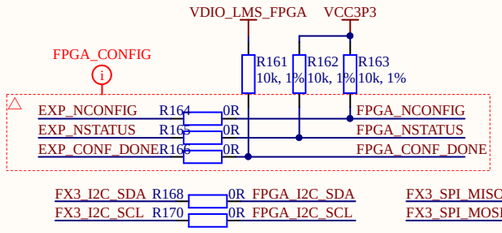
NF elements on sheet: R143, R155, R169, R174, R177, R178, R181, IC27, JMP1
Number of NF elements on sheet: 9

FX3 (USB3) core

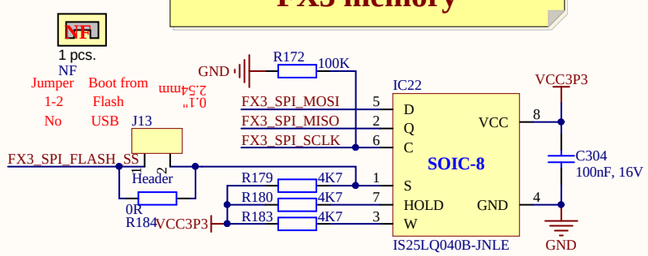




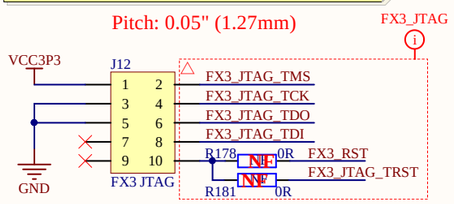




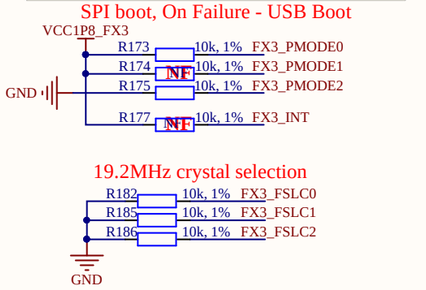
FX3 memory



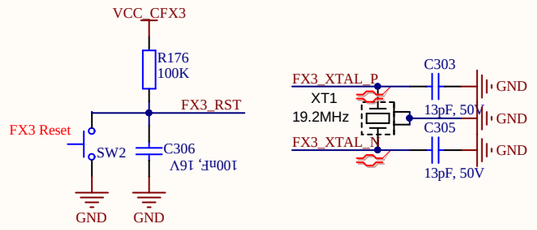
FX3 JTAG (10 pin)



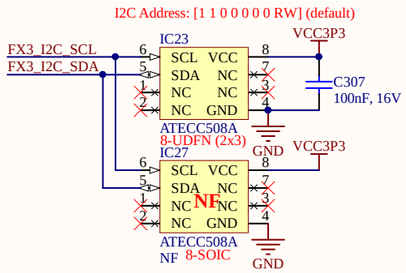
FX3 Config



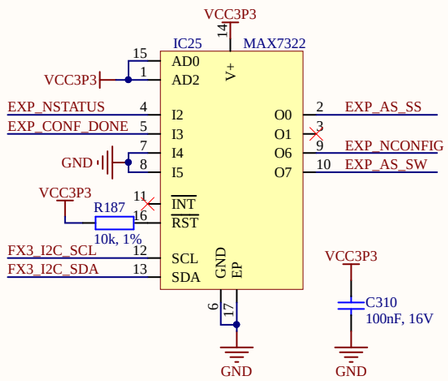
FX3 Misc



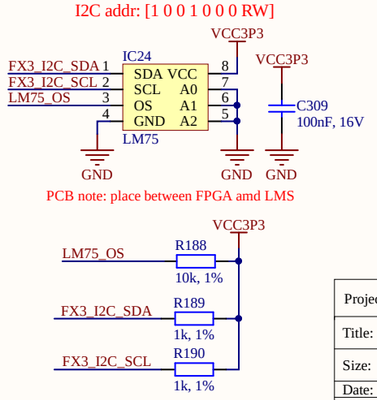
I2C secure key storage



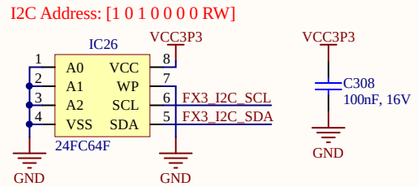
I2C Port Expander



I2C Temperature sensor



I2C EEPROM



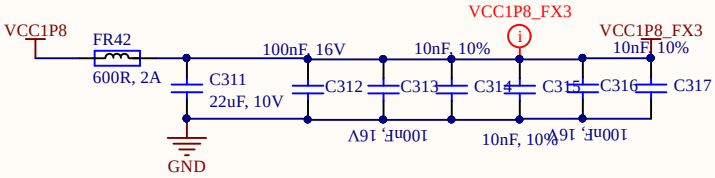
Project name:	*LimeSDR-CORE_SDR_1v1.PrjPcb*
Title:	*USB3.0 device*
Size: A3	Revision: v1.1
Date: 2018-11-28	Time: 10:51:59 Sheet 12 of 16
File: 12_USB3_0_device.SchDoc	

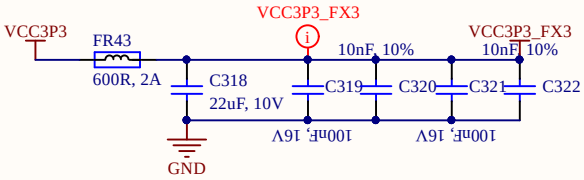
Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surray
United Kingdom

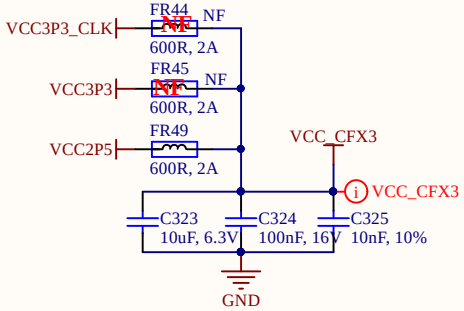
Lime microsystems

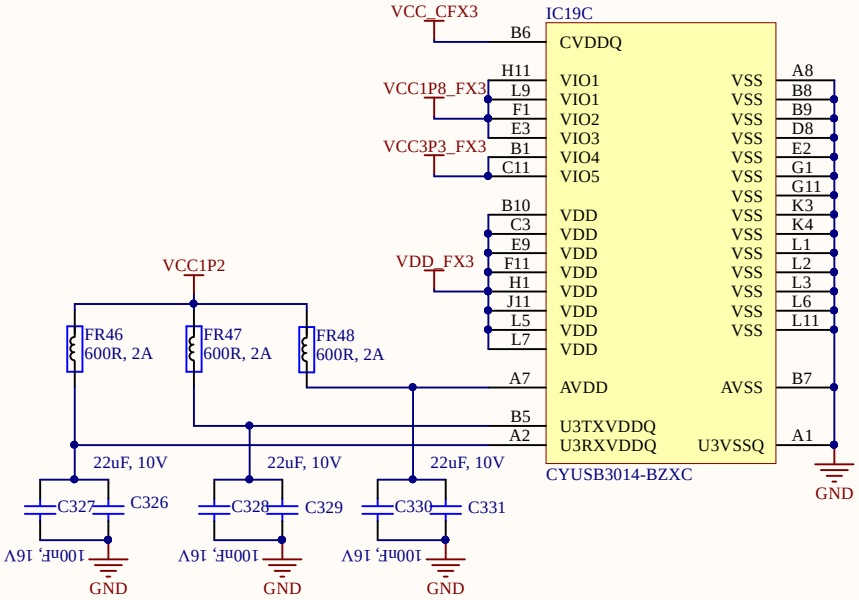
NF elements on sheet: FR44, FR45
Number of NF elements on sheet: 2

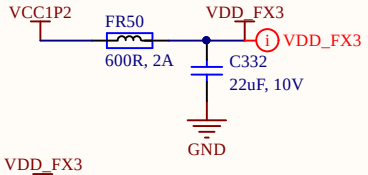
USB3 power

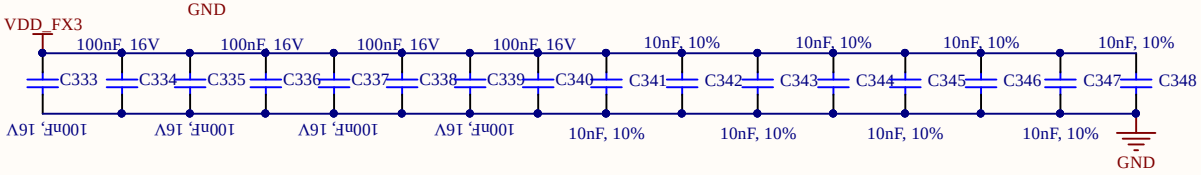












Project name: *LimeSDR-CORE_SDR_1v1.PrjPcb*			*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surray* *United Kingdom*
Title: *USB3.0 power*			
Size: A4	Revision: v1.1		
Date: 2018-11-28	Time: 10:52:03	Sheet13 of 16	
File: 13_USB3_0_power.SchDoc			

NF elements on sheet: XO3, R191, R192, R194, R200, R203, R204, R205, R206, R207, R208, R210, R223, R232, C393, C405, IC32

Number of NF elements on sheet: 17

Clock circuits

(VC)OCXO

PCB note: Place 100pF close to each Vddo pin.

Only one is fitted

VCC3P3_XO

FR51 600R, 2A

R196 0R

C352 10uF, 16V

C351 100nF, 16V

C353 100pF, 50V

XO_VC

XO1 VCOCXO

NC/VC Output

Vcc GND

U7475LF 30.72MHz

R195 0R

CLK_PATH

(VC)TCXO

XO2 VCTCXO1

VDD OUT

TRI-ST. T.S.

VC GND

E6245LF 30.72 MHz

R202 0R

R205 NF 0R NF

XO3

VDD

GND OUT

Vc

E5280LF 30.72MHz NF

R206 NF 0R NF

C371 1uF, 10V

C370 100nF, 16V

R207 NF 0R NF

XO4 VCTCXO2

VC FILTER RF OUT

VCO

VCC NC

NC

NC

GND NC

RTX5032A, 40.00MHz

R208 NF 0R NF

R209 22R

C373 1uF, 10V

C374 100nF, 16V

C375 18nF, 16V

Clock generator

I2C Address: [1 1 0 0 0 0 0 RW]

REF_CLK_OUT R200 NF 0R NF

R201 0R

IC29 20-QFN Si5351C

VCC3P3_CLK VCC1P8

CLKIN VDD

VDDOA VDDOB VDDOC VDDOD

OEB

SDA SCL

INTR

CLK0 CLK1 CLK2 CLK3 CLK4 CLK5 CLK6 CLK7

XA XB

GND

R204 NF 0R NF

SI_CLK0 SI_CLK1 SI_CLK2 SI_CLK3 SI_CLK4 SI_CLK5 SI_CLK6 SI_CLK7

SI_CLK

FX3_I2C_SDA

FX3_I2C_SCL

C361 10pF, 25V

SI5351_XTAL_P

XT2 25MHz

SI5351_XTAL_N

C372 10pF, 25V

VCC3P3_CLK

C378 100nF, 16V

C379 100nF, 16V

C380 100nF, 16V

VCC1P8

C376 100nF, 16V

C377 100nF, 16V

Only one is fitted

FPGA_CLK_OUT R191 NF 0R NF

REF_CLK_IN R192 NF 0R NF

SI_CLK4 R194 NF 0R NF

CLK_PATH

C350 100nF, 16V

C349 100nF, 16V

R198 49.9R, 1%

C354 100nF, 16V

Clock buffer

VDIO_LMS_LMK

VCC3P3_LMK

+1.8V_DIG_LMK

R193 0R

IC28 LMK00105

CLKin CLKin*

OE SEL

OSCin OSCout

Vdd Vdd

Vddo Vddo

Vddo Vddo

Vddo Vddo

CLKout0 CLKout1

CLKout2 CLKout3 CLKout4

GND

R197 0R

R199 0R

TxPLL_CLK

RxPLL_CLK

REF_ADF

LMK_CLK

REF_CLK_OUT

C355 13pF, 50V

C356 13pF, 50V

VDIO_LMS_FPGA

FR52 600R, 2A

C357 1uF, 10V

C358 100nF, 16V

C359 100pF, 50V

C360 100pF, 50V

PCB note: Place 100pF close to each Vddo pin.

VCC3P3_LMK VDIO_LMS_FPGA

R203 NF 0R NF

VCC3P3_CLK

FR53 600R, 2A

VCC3P3_LMK

C363 1uF, 10V

C364 100nF, 16V

C365 100pF, 50V

C366 100pF, 50V

PCB note: Place 100pF close to each Vdd pin.

VCC1P8

FR54 600R, 2A

+1.8V_DIG_LMK

C362 1uF, 10V

C367 100nF, 16V

C368 100pF, 50V

C369 100pF, 50V

XO VC DAC (16 bit)

VCC3P3_XO

FR56 600R, 0.27A

C387 1uF, 10V

C388 100nF, 16V

C389 100pF, 50V

IC30 AD5662

Vdd Vout

Vref

SYNC Vfb

SCLK

DIN

GND

TCXO_DAC_VREF

FPGA_SPI1_DAC_SS_R

FPGA_SPI1_SCLK_R

FPGA_SPI1_MOSI_R

FPGA_SPI1_DAC_SS R211 49.9R, 1% FPGA_SPI1_DAC_SS_R

FPGA_SPI1_SCLK R212 49.9R, 1% FPGA_SPI1_SCLK_R

FPGA_SPI1_MOSI R213 49.9R, 1% FPGA_SPI1_MOSI_R

R216 1k, 1%

R217 0R

XO_VC

C393 NF 100nF, 16V NF

C397 1nF, 50V

XO DAC (8 bit)

VCC2P5

R222 3k, 1%

R223 NF 1k, 1% NF

R224 10k, 1%

Vref=2.538V

TCXO_DAC_VREF

C402 1uF, 10V

C403 100nF, 16V

IC32

SCLK VOUT

SDIN

SYNC NF

VDD GND

AD5601BKSZ-REEL7 NF

FPGA_SPI1_SCLK_R 2

FPGA_SPI1_MOSI_R 3

FPGA_SPI1_DAC_SS_R1

VCC3P3_XO

FR57 600R, 2A

C406 100nF, 16V

R231 3k, 1%

R232 NF 10k, 1% NF

Vout=2.538V

XO_VC

C405 NF 100nF, 16V NF

Phase detector

VCC3P3_CLK

FR55 600R, 0.27A

C381 100nF, 16V

C382 100nF, 16V

C383 100pF, 50V

C384 100pF, 50V

C385 100pF, 50V

C386 100pF, 50V

REF_ADF

R214 49.9R, 1%

R215 10R, 5%

C392 100pF, 50V

C394 100nF, 16V

C390 100pF, 50V

C391 100pF, 50V

R218 1k, 1%

IC31 ADF4002

CE Vp CP MUXOUT Rset CPGND

DVdd DVdd AVdd AVdd

DGND DGND AGND AGND AGND

REFin RFinA RFinB CLK DATA LE

ADF_MUXOUT

XO_VC

R221 0R

R219 470R, 0.5%

C398 22pF, 50V

C399 22pF, 50V

C400 22pF, 50V

R227 330R, 5%

R225 10k, 1%

R226 10k, 1%

C404 10pF, 25V

C395 1nF, 50V

C396 1nF, 50V

REF_CLK_IN

R220 49.9R, 1%

C401 220pF, 10%

R228 49.9R, 1% FPGA_SPI1_SCLK

R229 49.9R, 1% FPGA_SPI1_MOSI

R230 49.9R, 1% FPGA_SPI1_ADF_SS

REF CLK OUT

REF_CLK_OUT R210 NF 0R NF

J14 U.FL/MMCX

REF CLK IN

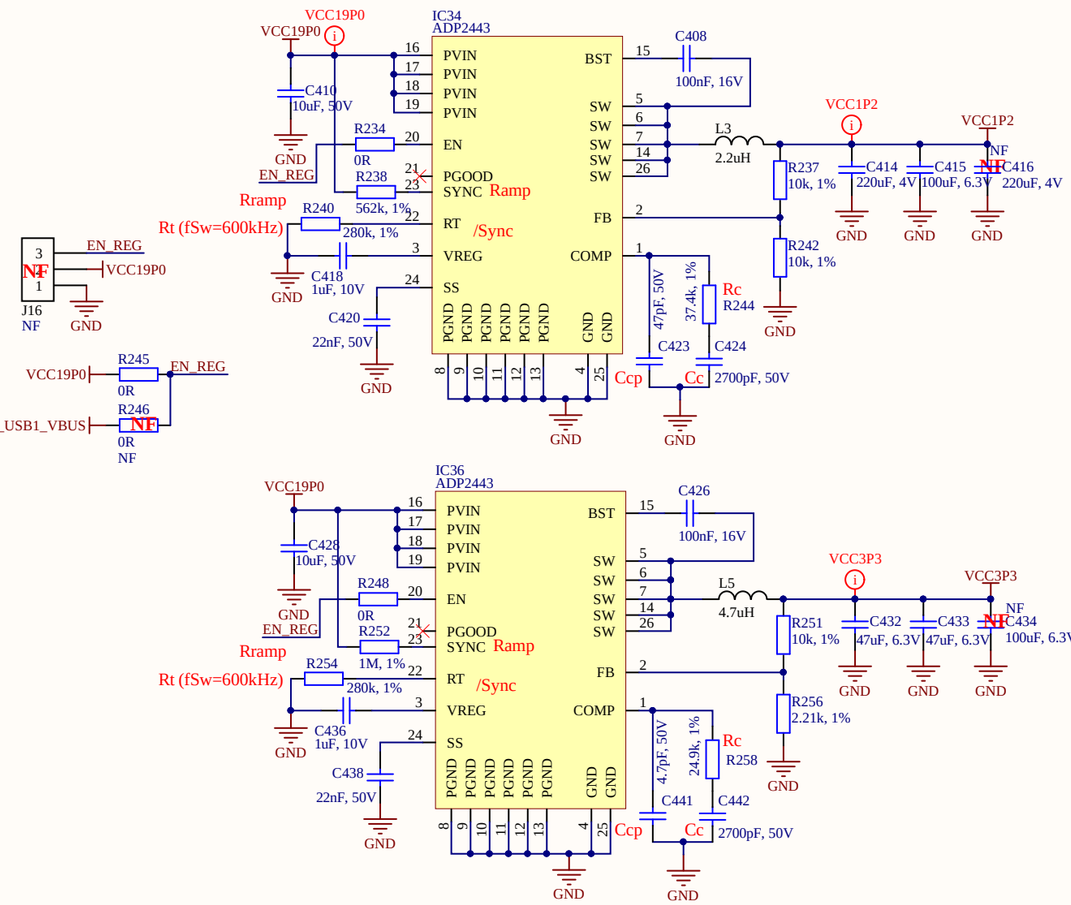
J15 U.FL/MMCX

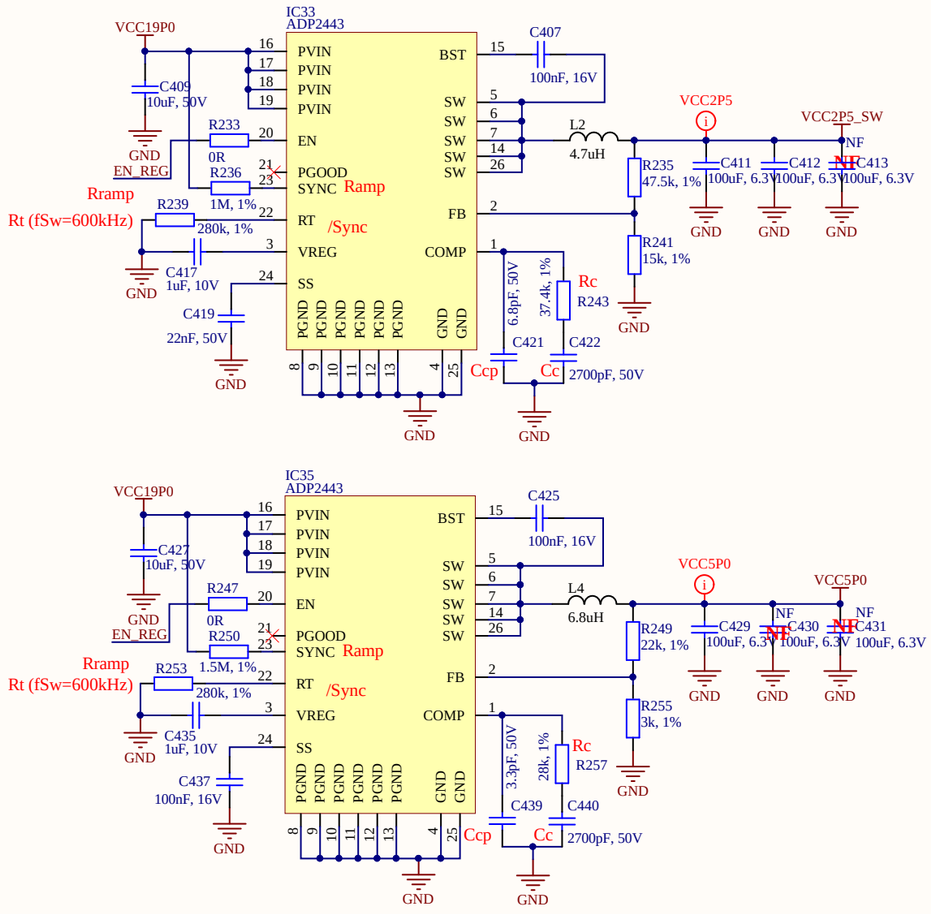
XO freq	30.72MHz	40.00MHz
C398	470nF	60nF
C99	68pF	4.6nF
R227	5.1k	200k

Project name:	LimeSDR-CORE_SDR_1v1.PrjPcb	
Title:	Clocks	Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Revision: v1.1	
Date: 2018-11-28	Time: 10:52:07	Sheet 14 of 16
File: 14_Clocks.SchDoc		

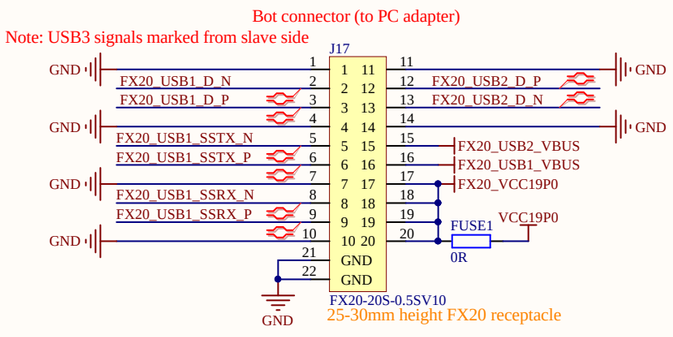
NF elements on sheet: C413, C416, C430, C431, C434, R246, J16
Number of NF elements on sheet: 7

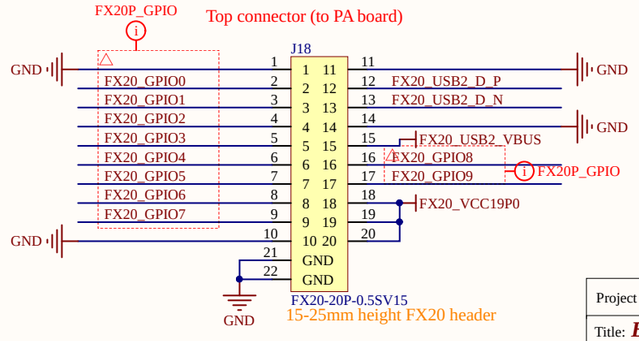
Board power circuits 1





Board to board connectors (FX20)



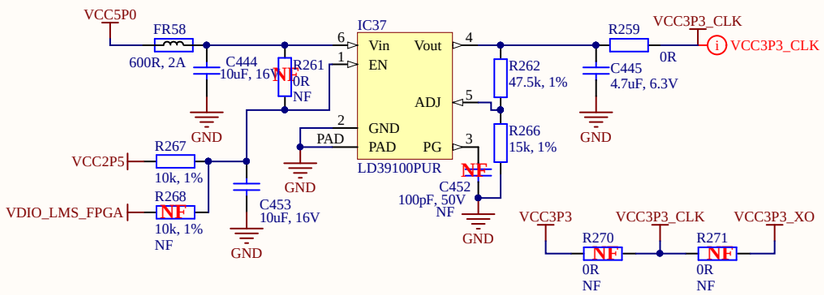


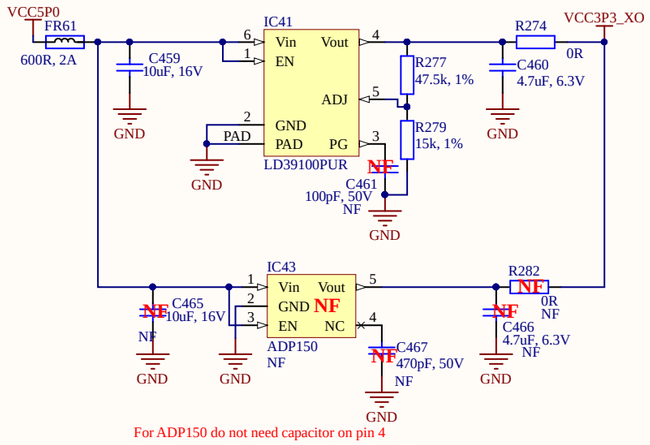
Project name:	*LimeSDR-CORE_SDR_1v1.PrjPcb*		
Title:	*Board power supply 1*		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v1.1		
Date: 2018-11-28	Time: 10:52:12	Sheet 15 of 16	
File: 15_Power1.SchDoc			

NF elements on sheet: R260, R261, R270, R271, C452, C461, C465, IC43, C466, C467, R282, R284, R288, R290, FAN1, MECH13-MECH15
Number of NF elements on sheet: 19
Total number of NF elements on all sheets: 92

Board power circuits 2

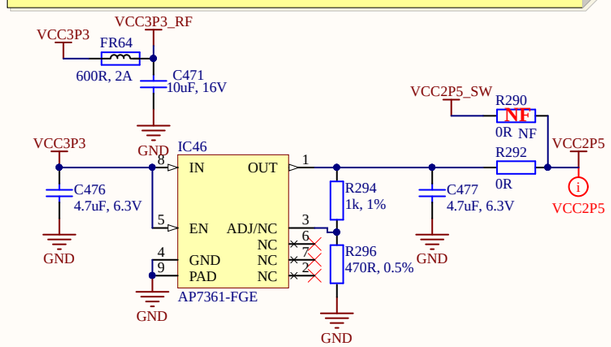
Clock network power

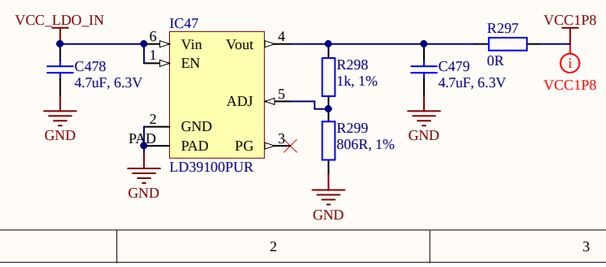




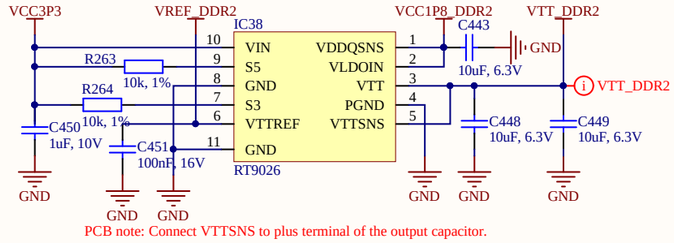
For ADP150 do not need capacitor on pin 4
Possible to use TC1185-3.3VCT713 LDO with bypass capacitor on pin 4

Misc power

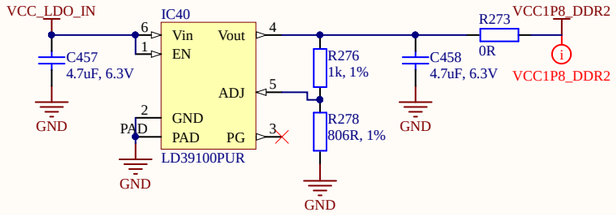




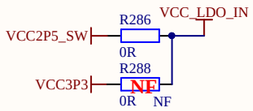
DDR2 power



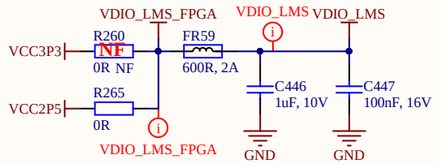
PCB note: Connect VTTSNS to plus terminal of the output capacitor.

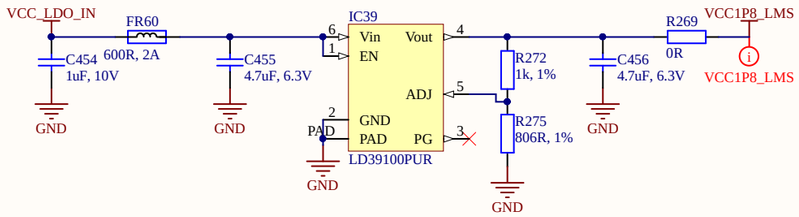


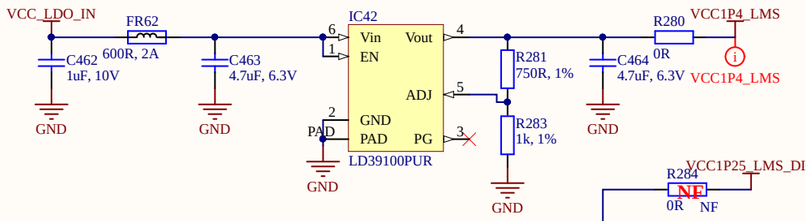
LDO power source

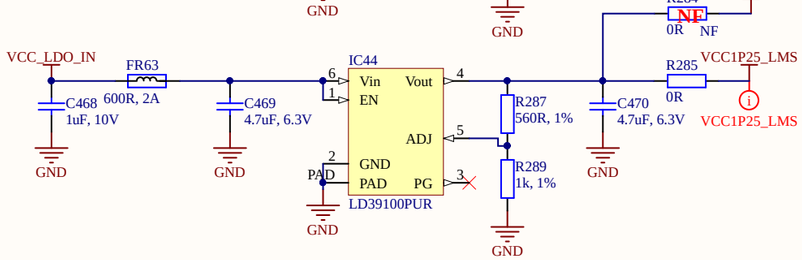


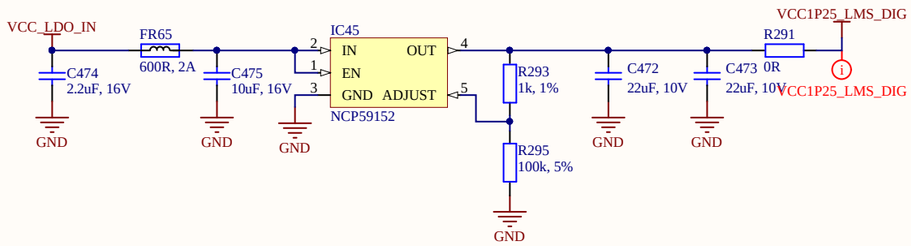
LMS power





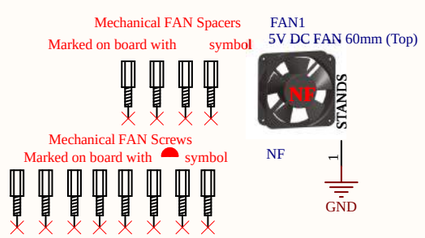




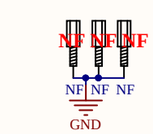


Mechanical FAN Spacers
Marked on board with symbol

Mechanical FAN Screws
Marked on board with symbol

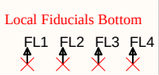


PCB standoffs
Marked on board with symbol



Global Fiducials

Local Fiducials Bottom



Project name:	*LimeSDR-CORE_SDR_1v1.PrjPcb*
Title:	***Board power supply 2***
Size: A3	Revision: v1.1
Date: 2018-11-28	Time: 10:52:17 Sheet 16 of 16
File: 16_Power2.SchDoc	

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Surrey Tech Centre
Guildford GU2 7YG
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United Kingdom

Lime microsystems